Readout ASICs for HEP experiments in the Faculty of Physics at AGH Experience&Potential

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People and Infrastructure

- Group at Faculty of Physics and Applied Computer Science AGH

➢ >5 researchers/ASIC designers +2 technicians + students

- Dedicated lab for microelectronics and detectors

➢Clean-room class ISO6

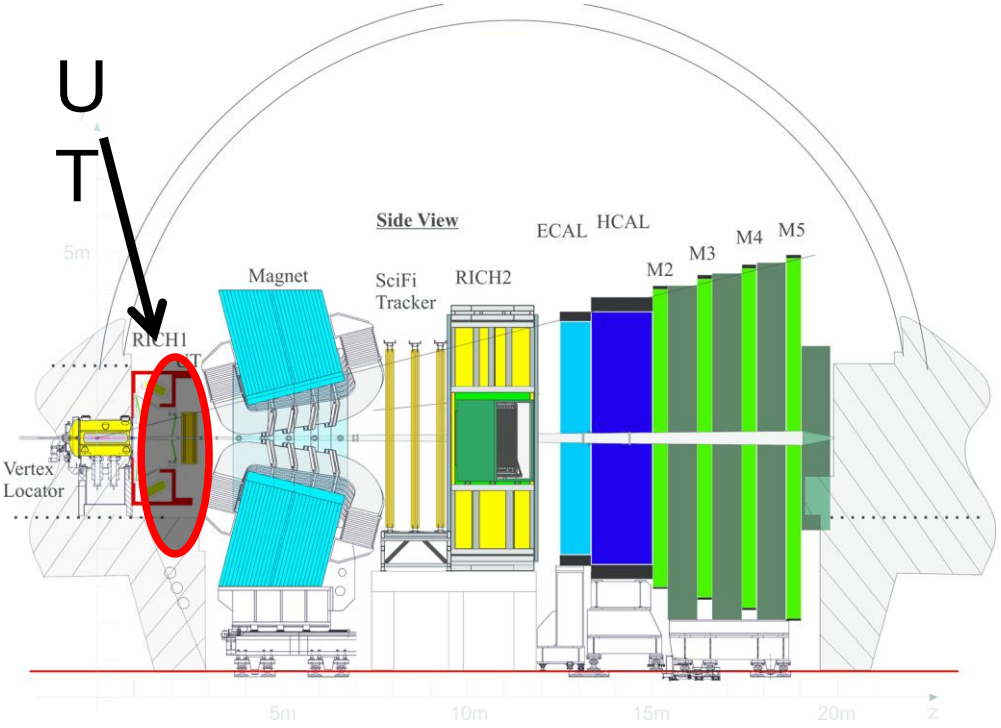
➢Equipment: probe-stations (e.g. *semi-automatic Cascade Summit 12000B-M with 8" chuck*), bonders (e.g. *F&S Bondtec 56XX*), semiconductor parameter analysers (e.g. *Agilent B1500A x 2*), spectrum/signal analysers (*Agilent 4395A, N9030A)*, scopes up to 80GS/s (e.g. *Agilent DSAV134A, 90804A*), generators (e.g. *Agilent 81150A, 81160A, N5172B*), semiconductor lasers (*Picoquant PDL 800-D with 660nm and 1060nm heads)*, radioactive sources, precise XYZ moving stages, High Voltage SMUs (e.g. *Keithley SMU237*), RLC meters (e.g. *Agilent E4980A)*, etc...

- ASIC/FPGA design tools

➢ Cadence tools, Synopsis, Mentor Graphics, Xilinx (FPGA design), Altium (PCB design)

Readout of Upstream Tracker (UT) LHCb-Upgrade I at LHC

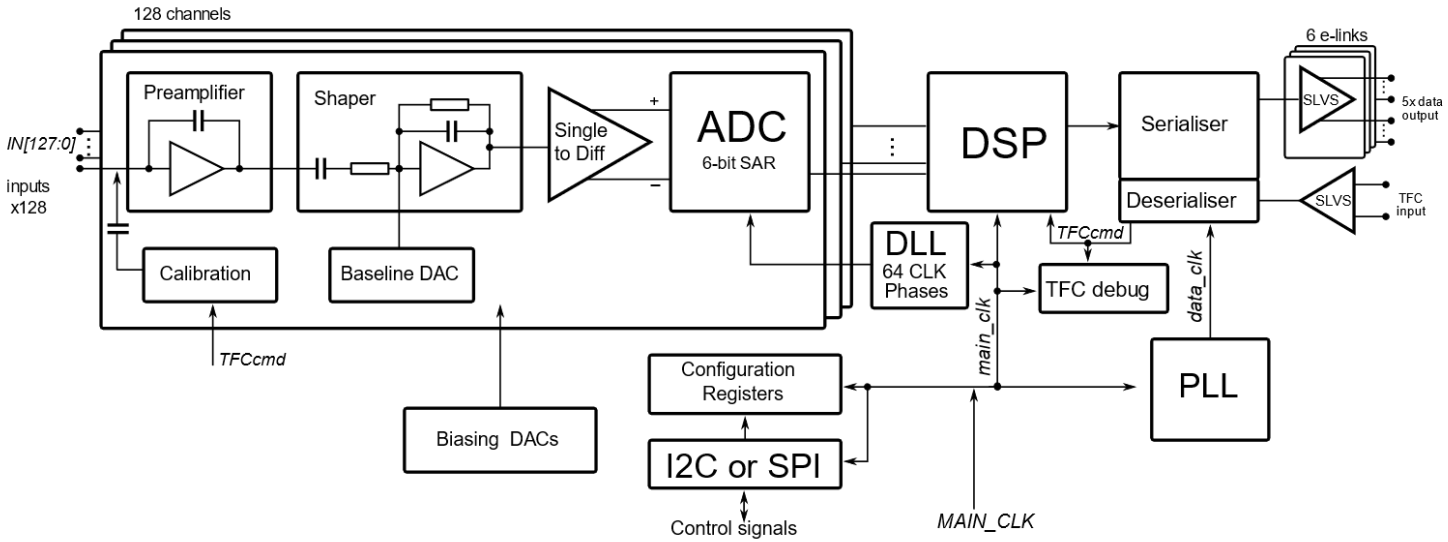
- In 2021 Upstream Tracker (UT) will replace the old Tracker Turicensis (TT)
- ~500 000 silicon strip detector channels will be readout with 40 MHz frequency
- The readout needs to be fast (Tpeak~25ns), with fast ADC in each channel, including on-chip DSP
- A dedicated chip – **S**ilicon **A**SIC for **L**HCb **T**racking – SALT, was designed
- AGH group is responsible for SALT development

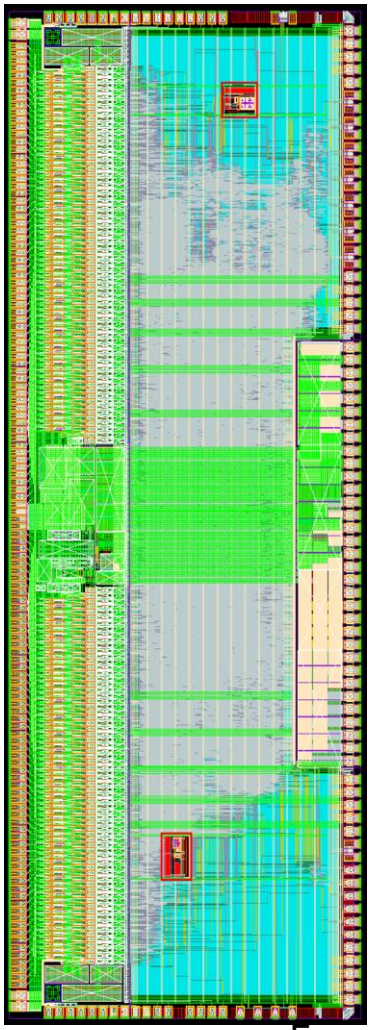


LHCb detector

K. Świentek, M. Firlej, T. Fiutowski, M. Idzik, J. Moroń, T. Szumlak "SALT – new silicon strip readout chip for the LHCb Upgrade", TWEPP2013 23-27 September 2013, Perugia Italy

Readout of Upstream Tracker (UT)
128-channel SALT ASIC in CMOS 130nm





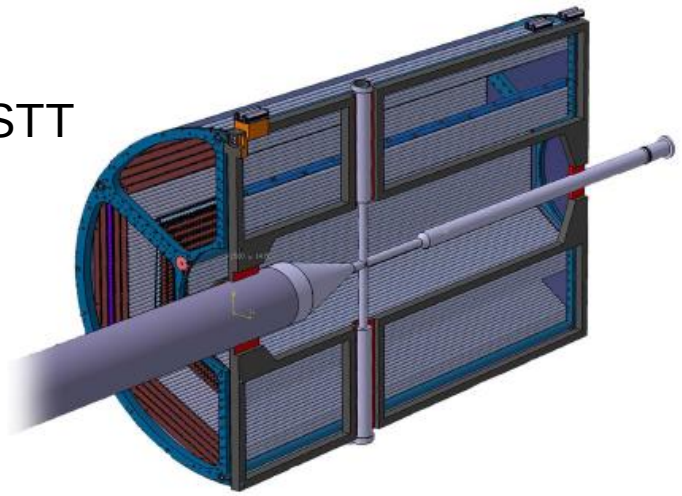
4.05mm x 10.9mm

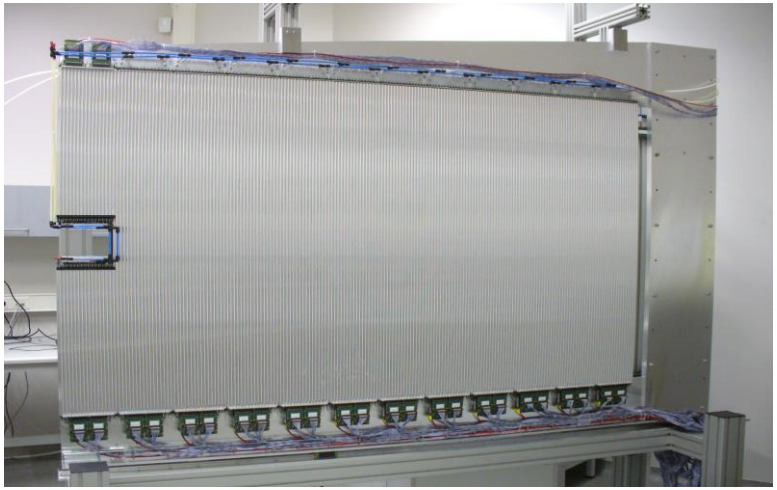
- SALT has 128 channels with front-end and 40MSps 6-bit ADC, followed by DSP, serialization and data transmission through fast links. A number of dedicated blocks like PLLs, DLL, monitoring circuitry, biasing DACs, calibration circuitry, I2C, SLVS, is needed to assure the required functionality.
- Group from AGH toke full responsibility for development of a very complex 128-channel readout ASIC
- First time in HEP experiment a high speed (40MSps) ADC was implemented in each channel of complex readout ASIC

Front-end electronics for Straw Tube Trackers FT&STT detectors in PANDA experiment at FAIR

• PANDA tracking system includes Straw Tube Tracker (STT) and Forward Tracker (FT), both built with gasous straw tube detectors. Both need similar front-end electronics (~15000 channels).
• AGH group (together with UJ group) is responisible for the readout of FT&STT

STT

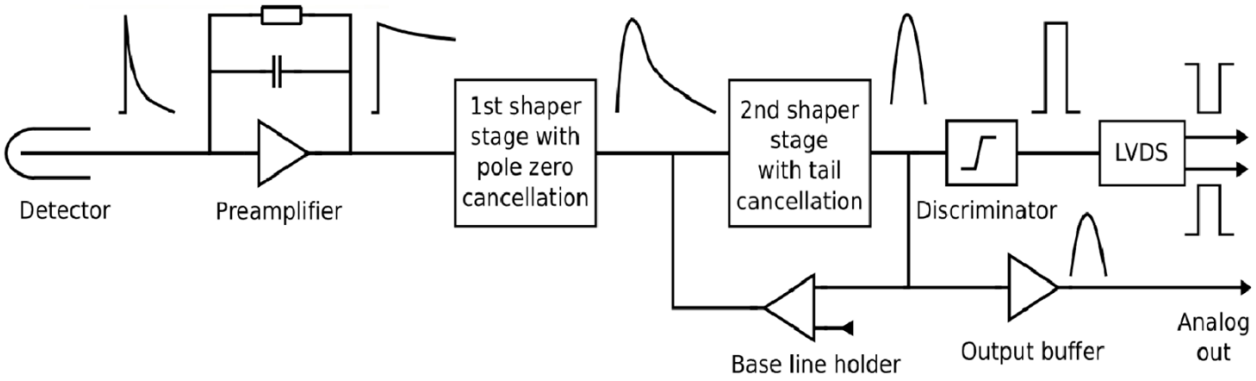


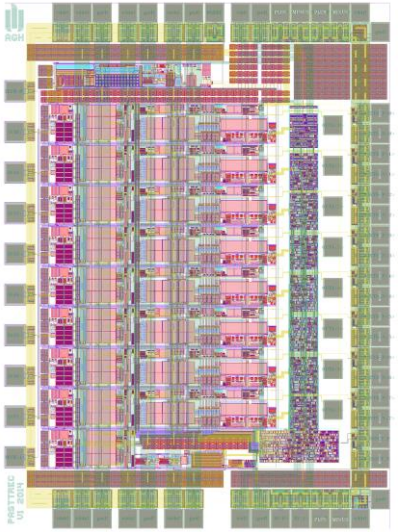


Straw tube module of FT detector

- ~5000 channels
- 1.5 m length, 10 mm diameter straws, C_{det}~25pF, Ar/CO2 (10%) gas mixture
- Max count rate ~1 MHz
- **Time and amplitude measurement performed by front-end ASIC**

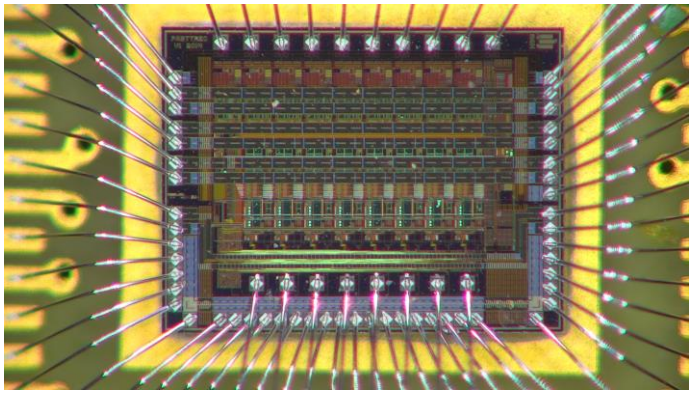
Front-end electronics for Straw Tube Trackers 8-channel PASTTREC ASIC in CMOS 350 nm





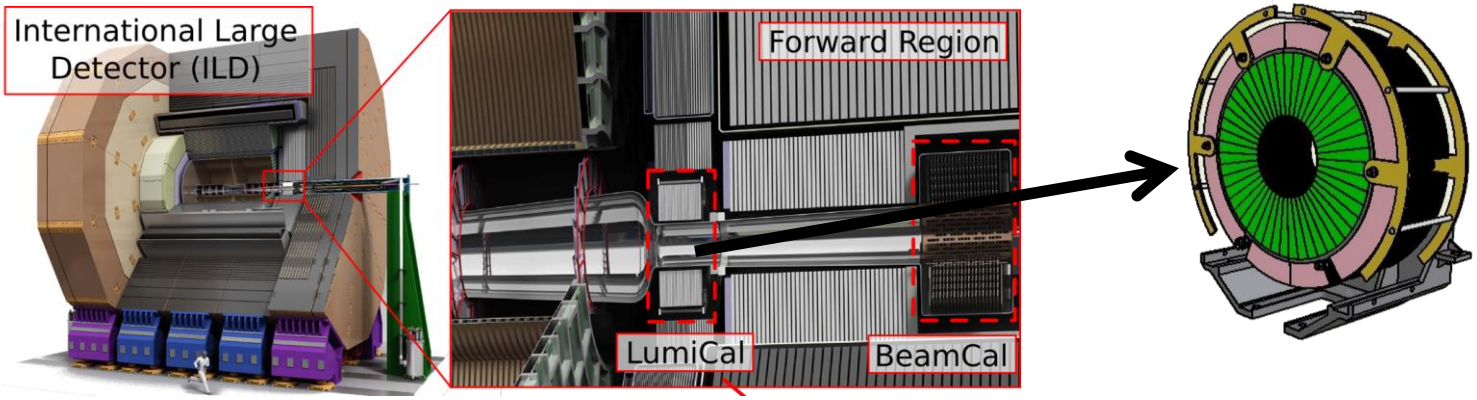
PASTTREC Layout

- PASTTREC ASIC contains 8 channels with fast Front-end (~20ns Tpeak), with TC circuit (Tail Cancellation for ion signal removal) and with binary output used for ToA and TOT measurements
- Recently PASTTREC readout was also adopted in HADES experiment for STS1, STS2 straw tubes and MDC detector

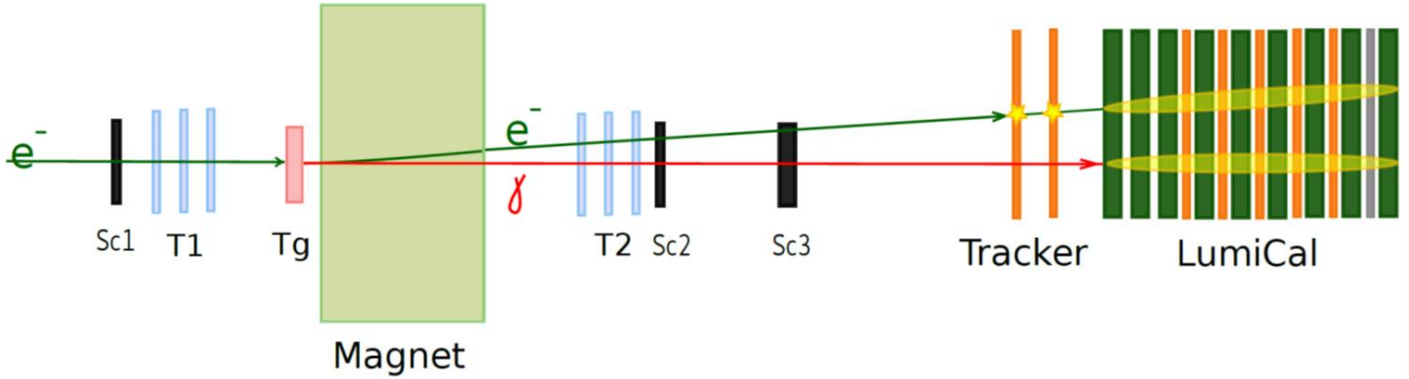


D. Przyborowski,T. Fiutowski, M. Idzik et al. "Development of a dedicated Front-end Electronics for Straw Tube Trackers in the PANDA Experiment", Journal of Instrumentation (JINST) in print...

Readout for luminosity calorimeter at Linear Collider R&D for LumCal calorimeter at ILC

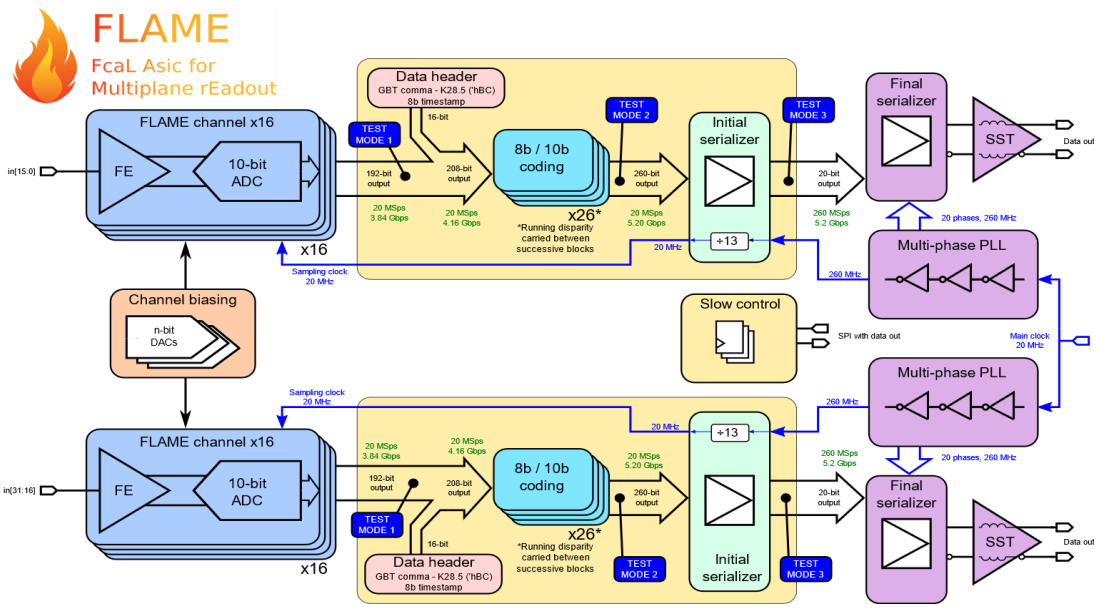


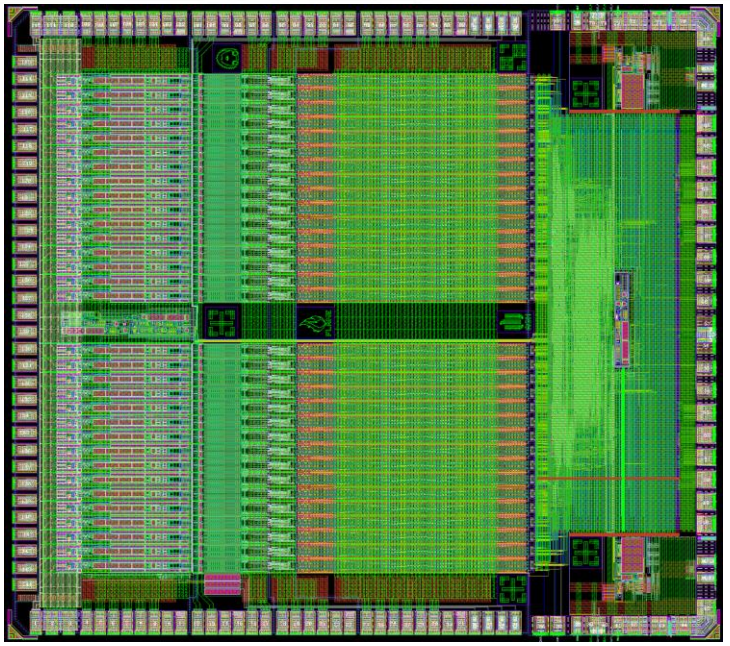
LumiCal serves for precise luminosity measurement in e+e- LC. It is built of 30 layers of sandwitch Si-W detector modules.



Within FCAL collaboration we have built and ...ts LumiCal prototypes consisting of up to ~10 layers angu...

Readout for luminosity calorimeter at Linear Collider 32-channel FLAME ASIC in CMOS 130nm

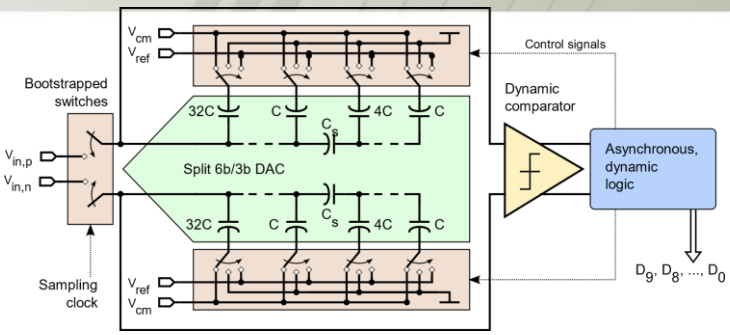




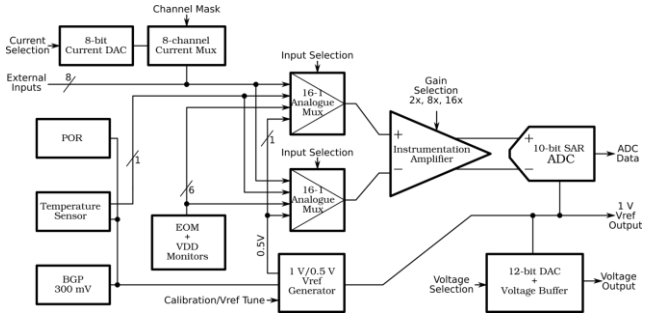
- AGH group has been developing luminosity detector (LumiCal) for ILC/CLIC, within FCAL collaboration. One of our main contributions is FLAME readout ASIC designed in CMOS 130 nm
- FLAME is a 32-channel ASIC with variable gain analog front-end and 10-bit ultra-low power (<0.5mW)ADC in each channel, followed by fast (~5Gbps) serializer and data transmitter
- FLAME operation was already verified at beam-tests at DESY

Other recent ASIC developments&contributions

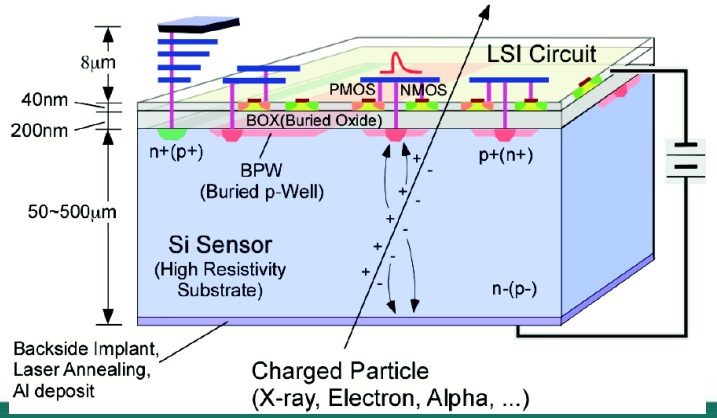
- We are contributiong to HGCAL in CMS to HGCROC readout chip with high speed 40MSps) ultra-low power (<1mW) 10-bit ADC in CMOS 130 nm



- We have contributed to lpGBT high speed data concentrator for HEP experiments developed at CERN with precise monitoring system in CMOS 65 nm



- We have developed and used in CLICdp beam-tests prototype monolithic pixel detectors in SOI CMOS 200 nm process



Summary

- The group from faculty of physics at AGH has been developing dedicated readout ASICs for HEP experiments for more than 20 years

- Several technologies have been used for ASIC design: CMOS 350nm, SOI CMOS 200nm, CMOS 130nm, CMOS 65nm. Soon CMOS 28nm should be started...

- Recent chips developed by the group: SALT for UT LHCb, FLAME for LumiCal at ILC, PASTTREC for FT/STT at PANDA, and contributions given to: HGCROC for HGCAL at CMS, lpGBT at CERN

Thank you for