

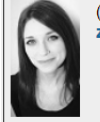


Krzysztof Kasinski, Robert Szczygiel on behalf of

Microelectronics Group Department of Measurement & Electronics

Agenda

- » Microelectronics Group
- » Selection of recent activities
 - SMX (for FAIR)
 - Other projects
- » Polish Microelectronic Industry

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CBM Detector Structure



Dipole Magnet

RICH
Ring Imaging Cherenkov

TRD
Transition Radiation Detector

TOF
Resistive Plate Chambers

MVD
Micro Vertex Detector

STS
Silicon Tracking System

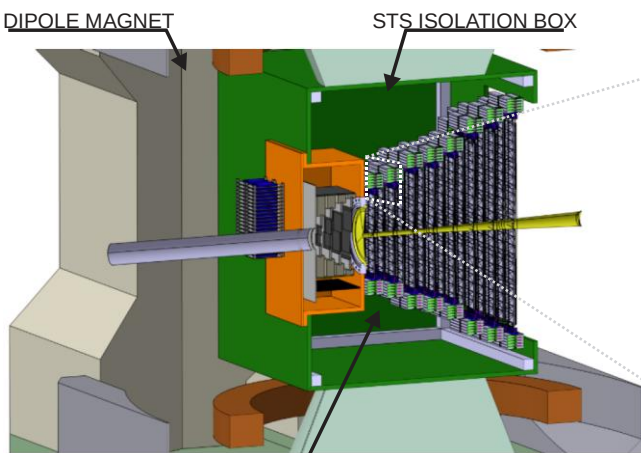
MUCH
Muon Detection System (parking pos.)

ECAL
Electro-Magnetic Calorimeter

PSD
Projectile Spectator Detector

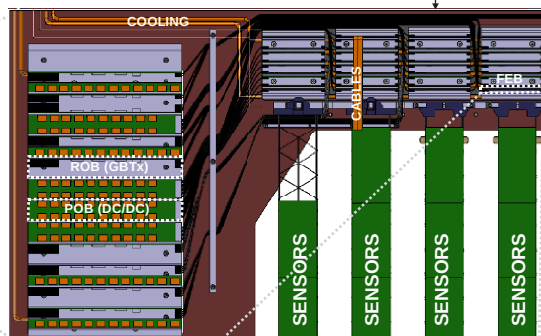
- Tracking acceptance:
 $2^\circ < \theta_{\text{lab}} < 25^\circ$
- Free streaming DAQ
- $R_{\text{int}} = 10 \text{ MHz (Au+Au)}$
- $R_{\text{int}} \approx 0.5 \text{ MHz}$
full bandwidth:
Det. – Entry nodes
reduced bandwidth
Entry nodes – Comp. farm
- with
 $R_{\text{int}} (\text{MVD}) = 0.1 \text{ MHz}$
- Software based event selection

STS



8 STS DETECTOR STATIONS

CORNER OF THE SINGLE STATION

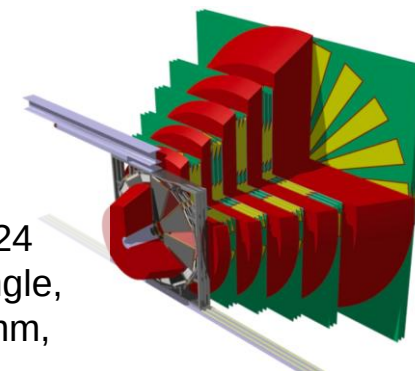


STS metrics:

- >1 790 000 channels
- >14 000 ASICs
- 1752 FEBs
- 600 ROB s, 78 DPB s

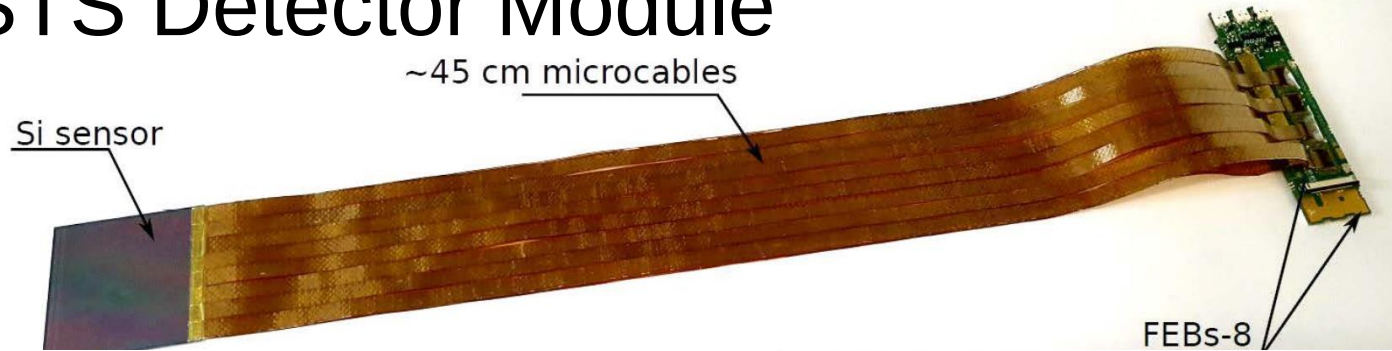
double-sided, micro-strip, 1024 channels per side, 7.5° stereo angle, $58 \mu\text{m}$ pitch, lengths 20 - 120 mm, $300 \mu\text{m}$ thickness,

MUCH





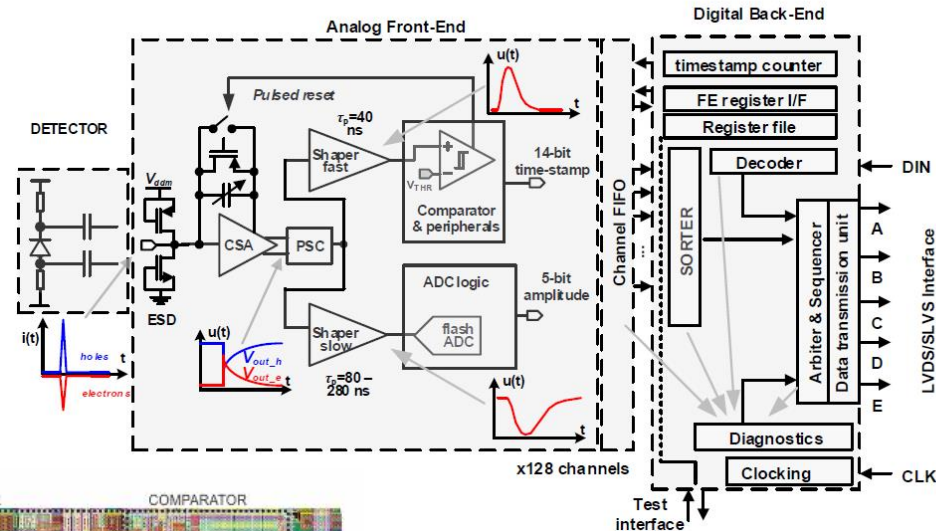
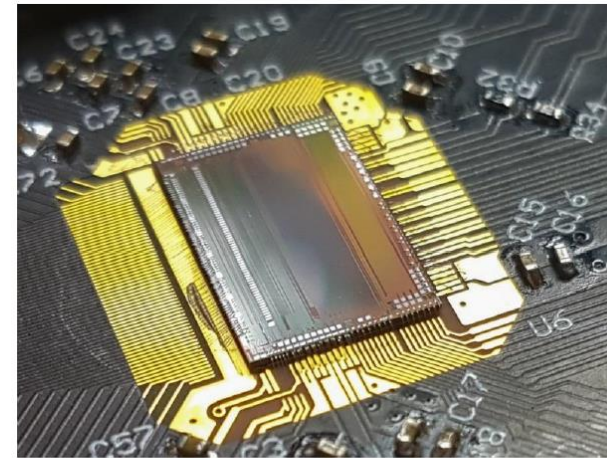
STS Detector Module



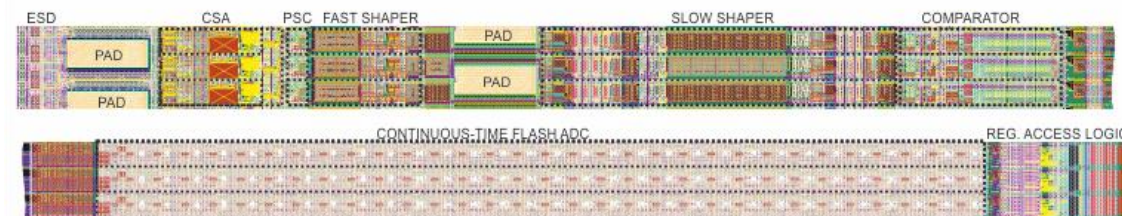
SMX2.2 chip

Features:

- Low power, self-triggering ASIC
- 128 channels + 2 test channels
- Time resolution ~ 5 ns
- Provides digitized hits with:
 - 5 bit Energy Resolution.
 - 14 bit Time stamp.
- Linearity range up to 15 fC
- Radiation hard layout



Parameter	Value
Process	180 nm CMOS MM/RF
Chip area	10.0 mm × 6.75 mm
Channel number	128 + 2 test
ADC bits	5
Input charge frequency	max. 500 kHz
Power	
Consumption:	0.6 – 1.2 W/chip
Uninitialized	1.023 W/chip @ $I_d=2$ mA
Initialized	8 mW/channel
Offset spread of fast channel	1.12 mV rms / 0.015 fC rms (after correction)
Offset spread of ADC [fC]	0.09 (before correction) [39] 0.02 (after correction)
Gain	
Fast shaper (STS)	73 mV/fC
Slow shaper (STS)	32.7 mV/fC
Gain spread:	
Fast shaper	0.8 %
Slow shaper	0.5 % (after calibration)
Slow shaper peaking time [ns]	90 / 180 / 262 / 332
Yield	>91% (146 ASICs tested on PCBs)





STS-XYTER 1.0 First full-size prototype. CBM-net compatible.

STS-XYTER 2.0 **Key changes:** back-end re-design for GBTx, multiple functional improvements. Added VREFT (common ADC threshold). STS/MUCH gain switching. Pogo-prober support.

STS-XYTER2.1 was fabricated on 2018 MPW run and thoroughly tested (LAB, mini-STs, irradiation sessions). **Key changes:** Removed MOS-based ESD protection, external ESD-TEST IC to test different protection approaches. Improved layout SEU/TID. VREFT improved resolution. Noise improvements (e.g, reduced series R on-chip). Biasing Improvements (even/odd discrepancies). STS/MUCH calibration support. Added on-chip diagnostic ADC.

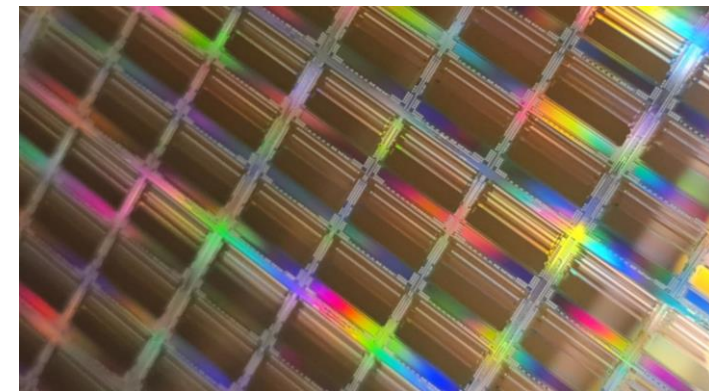


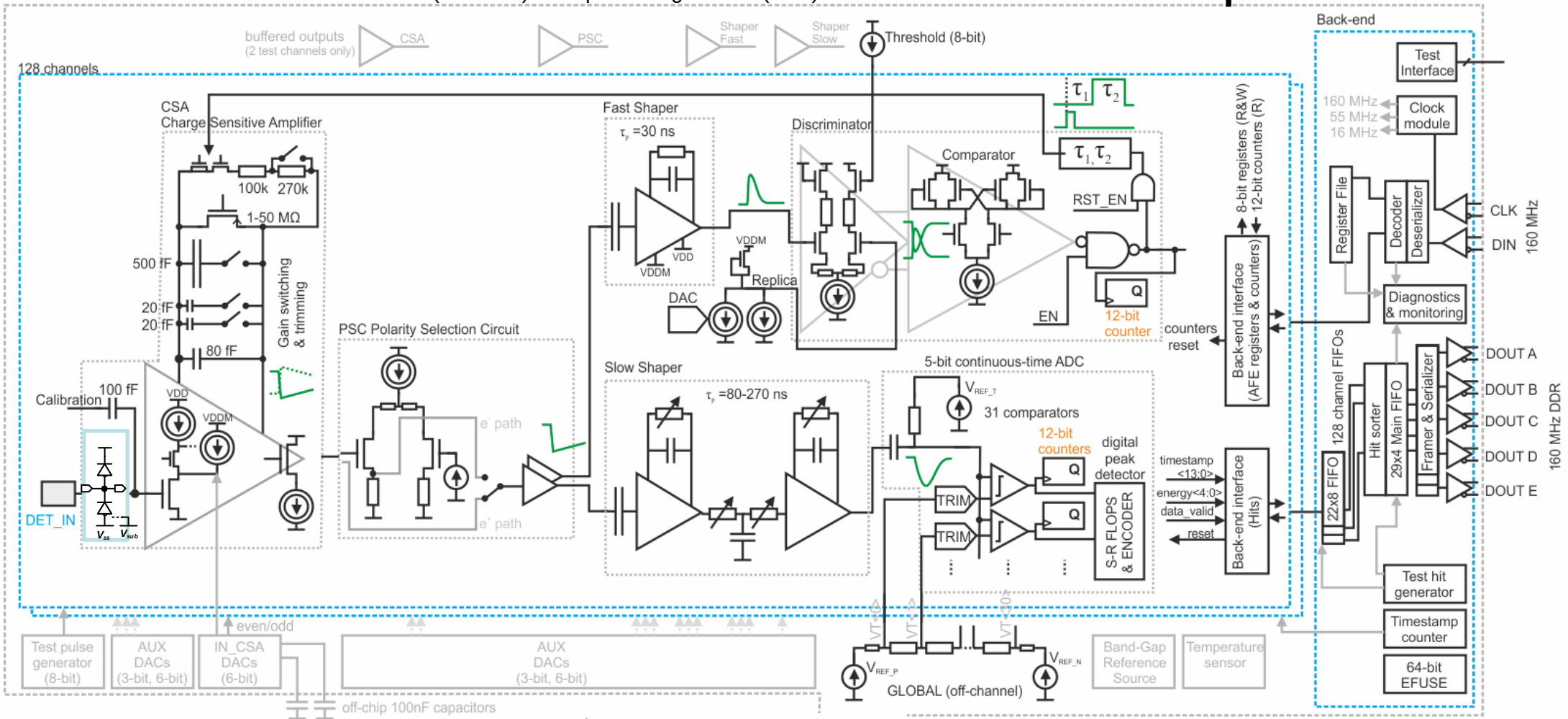
- **STS-XYTER2.2** Was fabricated and delivered Sept 2020. Full Reticle Engineering run.

Thoroughly tested (system-level, irradiation).

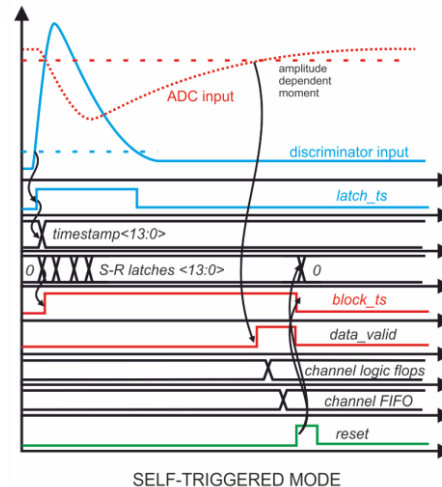
Changes:

- Diagnostic: more potentials added for on-chip monitoring (all VDDs)
- Layout: reduce risk of short during bonding of digital power
- Analog: implement diode-based ESD protection of the inputs
- Analog: reset timing modification
- Digital: fix read-back of 5 registers





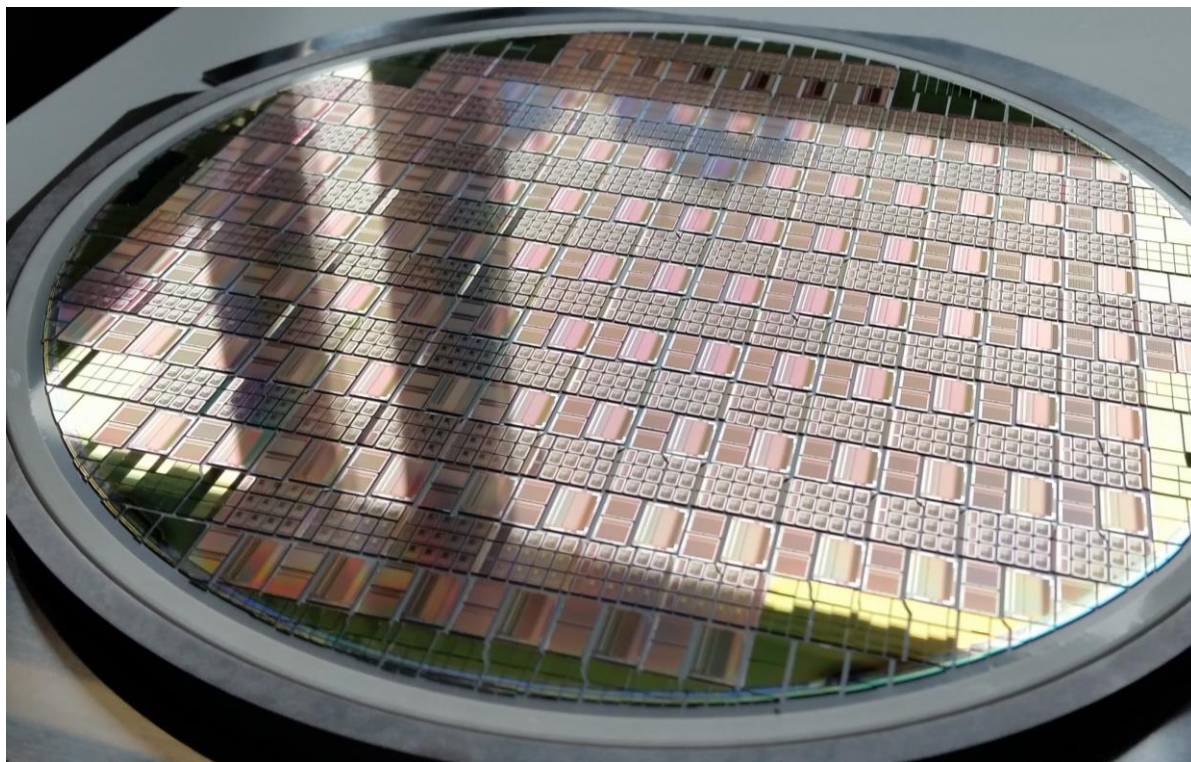
0-12 fC electrons & holes (STS)
 gain switching & trimming
 250 khit/s rate (pulsed reset)
 80-280 ns shaping time (slow path)
 time-walk corrected offline
 continuous-time ADC + peak det.
 P=8.5-10 mW/channel (incl. logic)



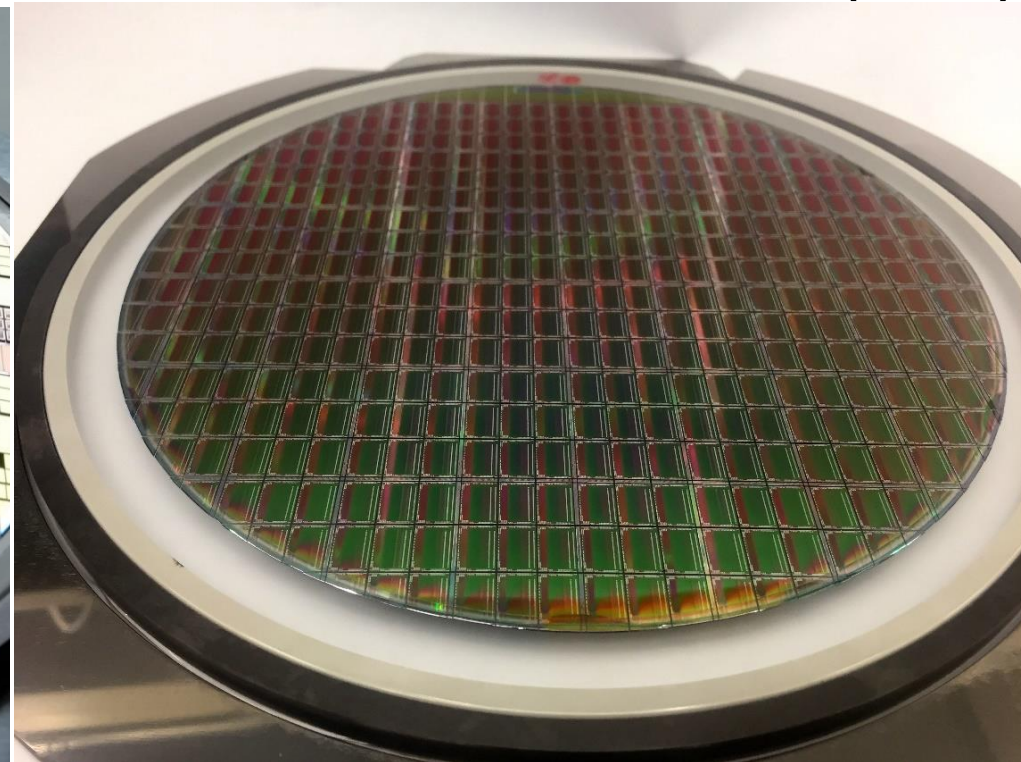
Back-end:

- control via synthesized reg & AFE DICE cells
- 9.41 – 47 Mhit/s/ASIC data BW
- dedicated protocol
- throttling, diagnostic features
- link loopback (multi-level)
- 64-bit e-fuse for traceability

GSI MPW

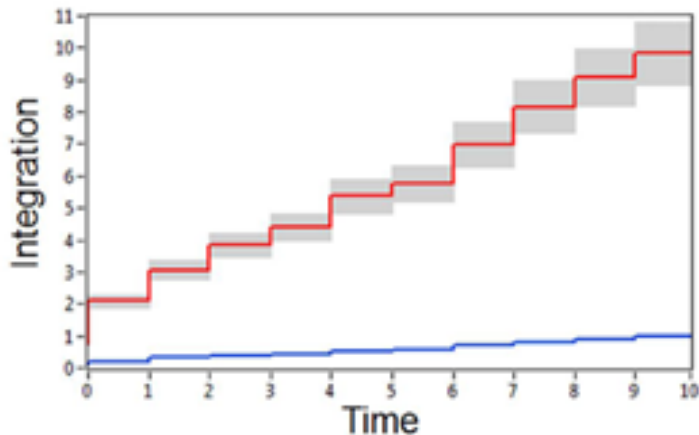
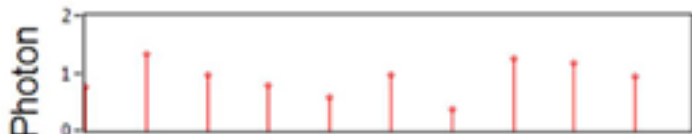
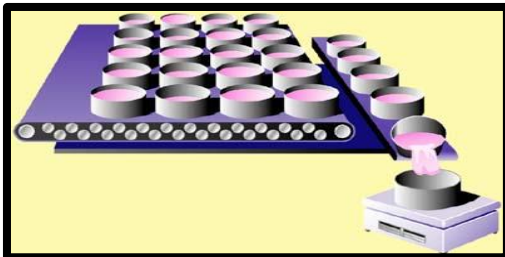
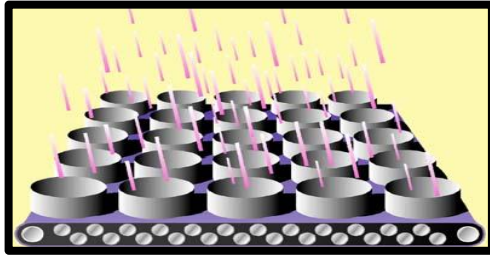


Dedicated Maskset for SMX (2020)



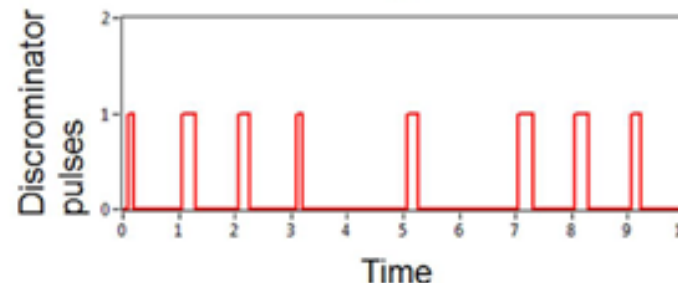
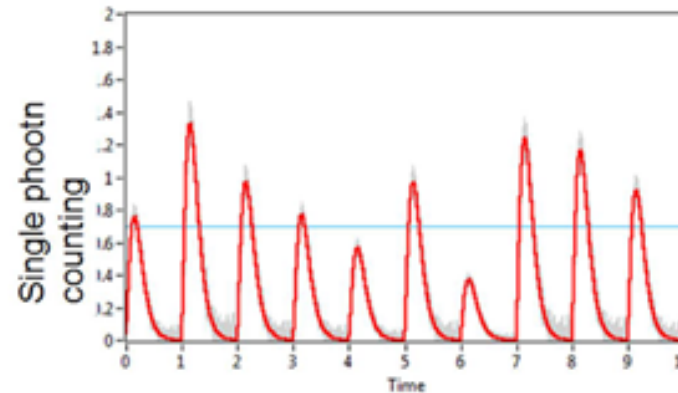
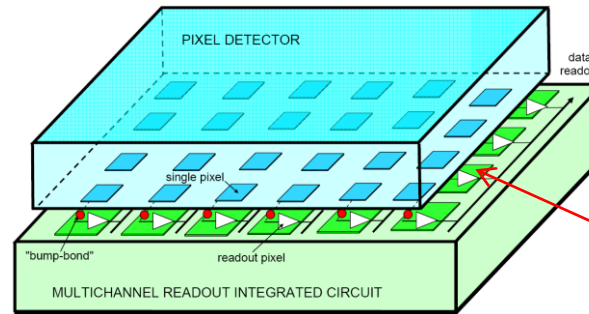
Two different types of readout IC for pixel detectors

Integration mode

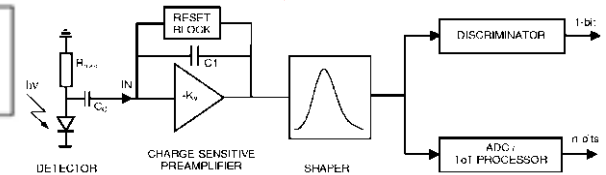


Noise are integrated together with signal

Single Photon Counting mode



Noise are cut from signals. Photons can be selected vs energy. Weak point – count rate

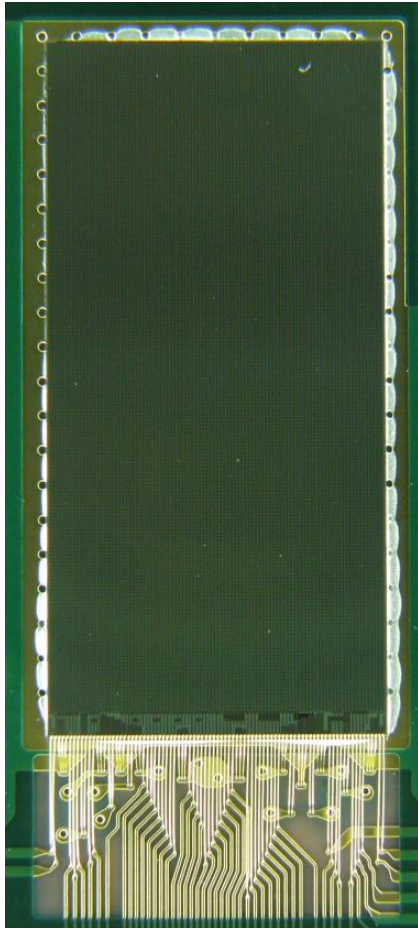


Trends:

1. High count rate
2. Small pixel area
3. Low noise
4. Energy measurements
5. Continuous readout
6. Large area detector

PXD18k chip – AGH, UST Krakow

PXD18k chip

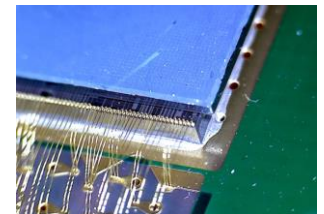


Summarized performance of the PXD18k IC.

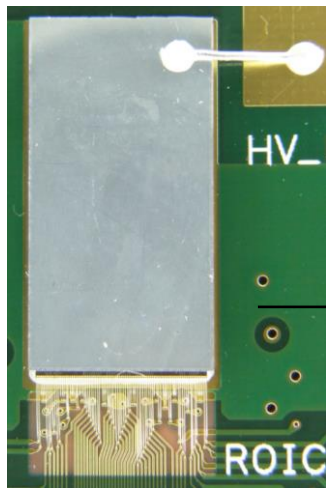
Parameter	
Technology	CMOS 180 nm
Die size	9.64 mm × 20 mm
Pixel dimensions	100 μm × 100 μm
Number of pixels	18,432
Supply voltage: core/LVDS	1.2 V/1.8 V
Power dissipation per pixel (analog)	23 μW
Peaking time	30 ns
ENC with bump-bonded detector	168 e ⁻ rms
Gain	42.5 μV/e ⁻
Offset spread (after correction with 7-bit)	< 1.8 mV rms
Dead time (paralyzable model)	172 ns
Number of discriminators per channel	2
Counters capacity	2 × 16-bit
Readout dead time—standard mode (eight outputs, 2 × 16 bits/pixel) and continuous mode	740 μs and 0
Frame rate in continuous mode (16 bit/4 bit)	2.7 kHz/7.1 kHz
Communication	LVDS standard with 100 MHz clock

192 x 96 = 18.432 pixels (100x100 μm²)
CMOS 180 nm, chip size 9.64x20 mm²

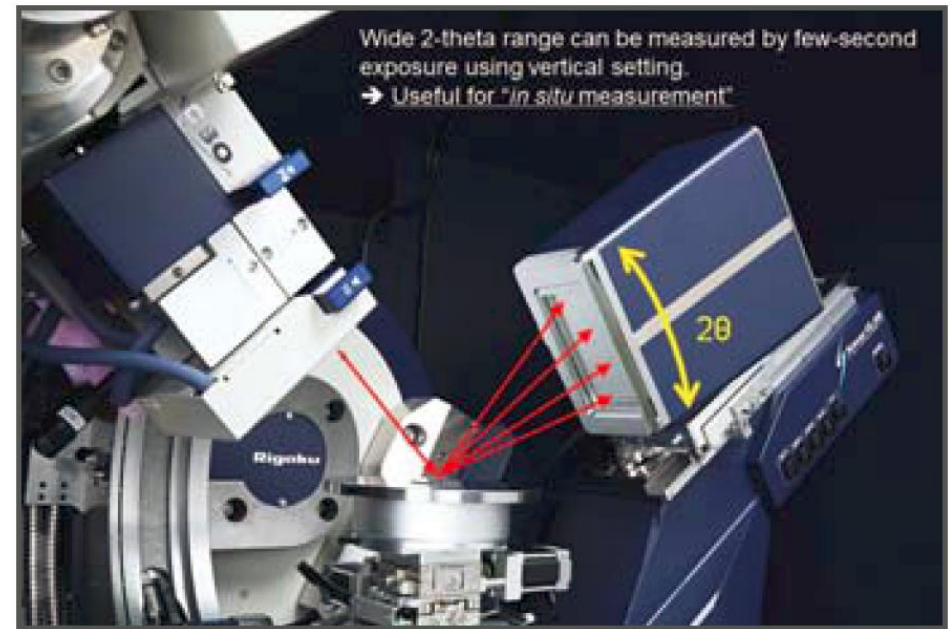
P. Maj, P. Grybos, R. Szczygiel, M. Zoladz, T. Sakumura, Y. Tsuji "18k Channels single photon counting readout circuit for hybrid pixel detector", NIM A, vol. 697, 2013, pp. 32-39.



AGH chip PXD18k is used in by Rigaku Corporation, Japan



x 16



Cement	Metals & alloys
Chemistry	Mining & refining
Coatings	Nanotechnology
Cosmetics	Petroleum & petrochemicals
Education	Pharmaceuticals
Environmental	Photovoltaic manufacturing
Food & food ingredients	Polymers, plastics & rubber
Forensics & conservation	Process control
Geology & minerals	Semiconductor manufacturing
Materials science	Synchrotrons & beamlines

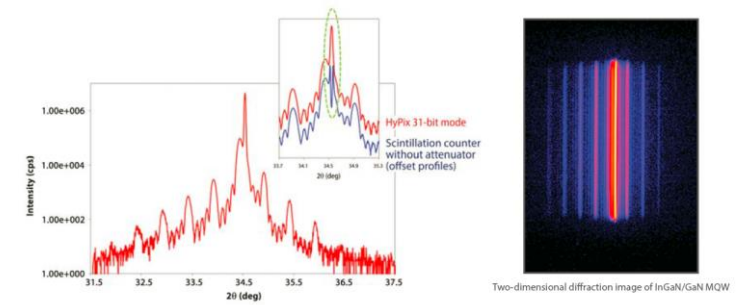
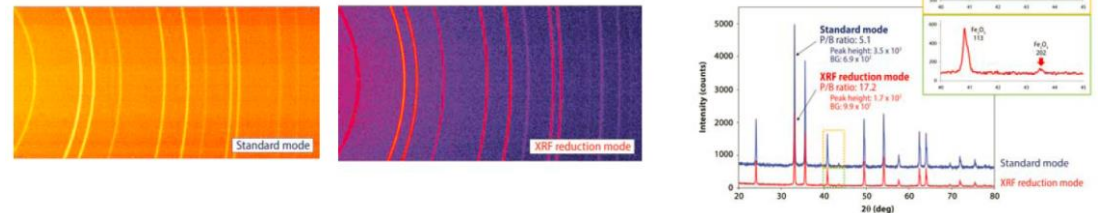


Figure 2. X-ray diffraction patterns of iron oxide powder, measured in standard mode and XRF reduction mode



Rigaku detectors based on PXD18k ASIC



HyPix-400

HyPix series



HyPix-6000HE



HyPix-9000



HyPix-3000



HyPix-Arc 150°



HyPix-54000

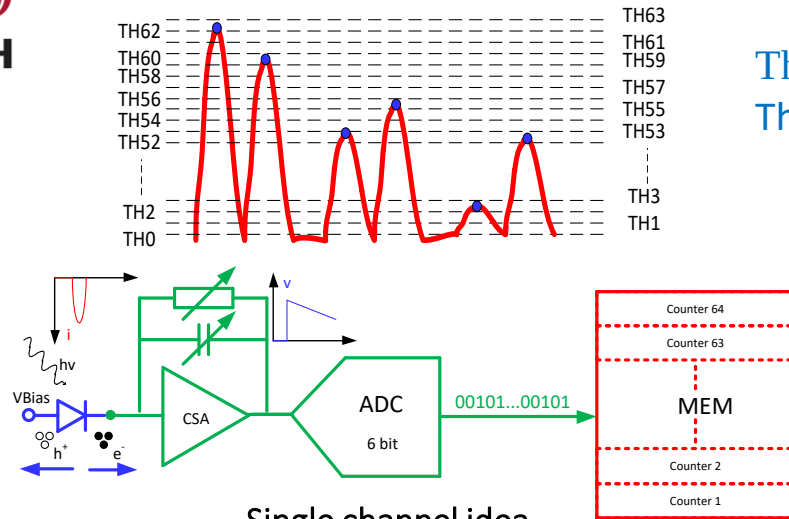
SPECTRUM 1k – Integrated Circuit for Medical Imaging Designed in CMOS 40 nm

P. Kmon, R. Szczygieł, R. Kłeczek, D. Górni, G. Węgrzyn, A. Niedzielska, K. Sitko, P. Drwal

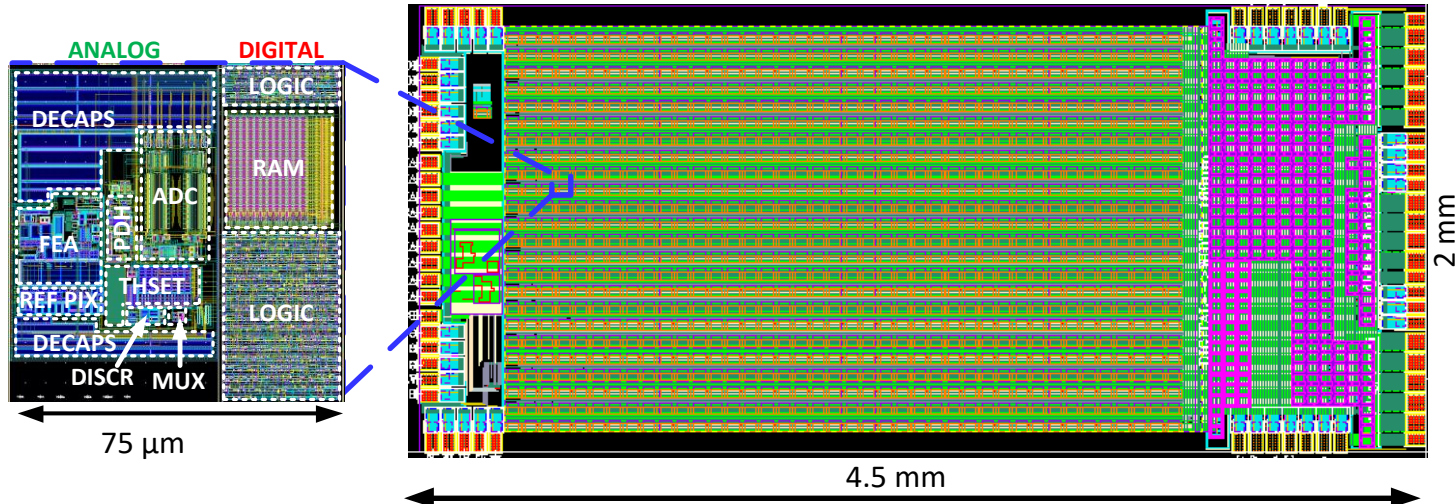
The idea was to build a chip composed of a CSA and an ADC in a single pixel.
The single pixel should store in counters based memory pulses' amplitudes.

Main IC parameters:

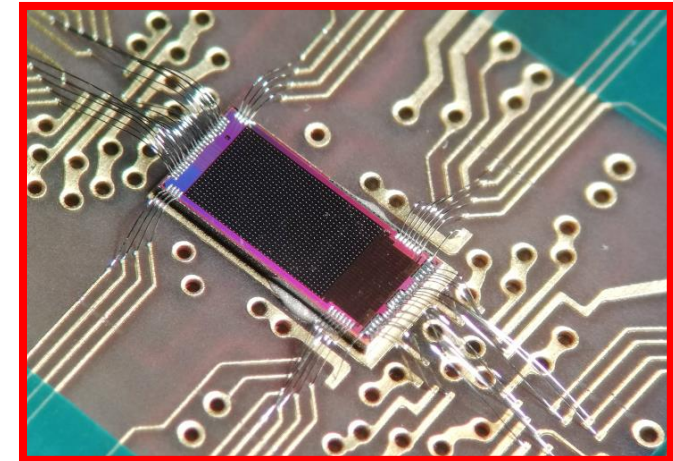
1. Input charge: electrons/holes, range: 2200 e^- - 32 000 e^-
2. Noise: 100 e^-_{RMS}
3. CSA output pulse time width controlled in 100 ns – 1 μ s range.
4. ADC architecture: 6 – bit SAR
5. Counters based memory: word length = 12 bit, words number = 64.
6. Pixel digital part synchronous with common global clock (100 MHz).
7. LVDS based readout system.



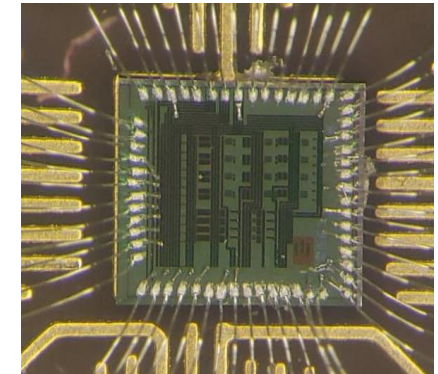
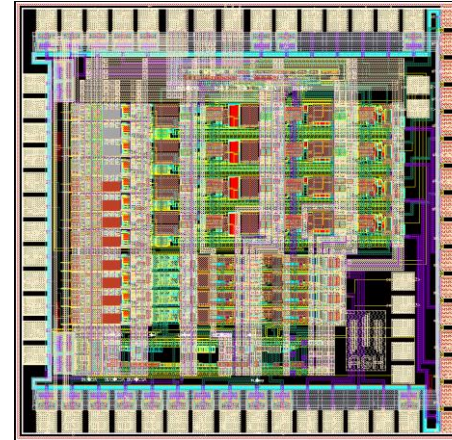
Single channel idea.



IC overview , single pixel's architecture details, and bonded chip photo.



- Area: mini@sic 180nm CMOS size, 1.5x1.5 mm
- 8 channels (4x single-ended, 4x pseudo-differential)
- Channel area:
 - single-ended: 0.057 mm²
 - pseudo-differential: 0.144 mm²
- External analog references
- Dissipated power - 88mW:
 - single-ended: ~ 4.62mW/ch,
 - pseudo-differential: ~ 12.31mW/ch
- Measured noise level (ENC) ~300 e- rms



Single-ended channel:

- Charge sensitive amplifier – CSA with configurable feedback: MOS transistor working as resistor or Krummenacher circuit
- Configurable shaping amplifier architecture

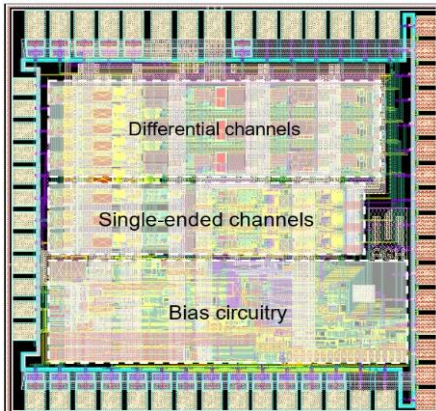
Channel type		Single-ended		Differential	
Input charge		Electrons	Holes	Electrons	Holes
CSA feedback type	MOS resistor	✓		✓	
	Krummenacher	For negative leakage For positive leakage		✗	
Slow Shaper architecture	CR-RC ²	✓		✓	
	CCP 3 rd order	✓		✓	
Polarity selection		Polarity Selection Circuit: ON	Polarity Selection Circuit: OFF	✗	

Differential channel:

- CSA and 1:1 scaled CSA replica, for power supply induced interference reduction
- Differential shaping amplifier
- Configurable shaping amplifier architecture

Channel type	Single-ended (mean ± sigma)	Differential (mean ± sigma)
CSA gain (mV/fC)	8.813 ± 0.383	9.425 ± 0.263
CSA peaking time (ns)	55.5 ± 2.976	57 ± 5.291
Slow Shaper gain (mV/fC)	33.75 ± 1.909	33.81 ± 1.28
Slow Shaper peaking time (ns)	94.25 ± 3.284	93 ± 2.582

- 180nm CMOS mini@sic
- Area: 1.5x1.5 mm
- 6 channels (3x single-ended, 3x pseudo-differential)
- Integrated DACs for references
- Integrated calibration circuit
- ENC: $\sim 350 \text{ e}^- \text{ rms}$ @ 5 pF input capacitance



Channel type	Single-ended	Differential
CSA average gain (mV/fC)	9.323 ± 0.134	9.723 ± 0.08
CSA average peaking time (ns)	49.905 ± 4.231	57.166 ± 4.759
Slow Shaper average gain (mV/fC)	32.123 ± 0.716	33.63 ± 1.139
Slow Shaper average peaking time (ns)	95.033 ± 2.261	94.75 ± 3.623
Fast Shaper average gain (mV/fC)	72.85 ± 1.735	79.443 ± 1.518
Fast Shaper average peaking time (ns)	48.203 ± 4.103	58.545 ± 6.064

Channel type		Single-ended		Pseudo-differential	
		Electrons	Holes	Electrons	Holes
CSA feedback type	MOS resistor	✓		✓	
	Krummenacher	For negative leakage		✗	
		For positive leakage			
Fast Shaper		✓		✓	
Slow Shaper architecture	CR-RC ²	✓		✓	
	CCP 3 rd order	✓		✓	
Polarity selection		Slow shaper – V _{ref} low Fast shaper - V _{ref} high	Slow shaper – V _{ref} high Fast shaper - V _{ref} low	Slow shaper - switch at the shaper input Fast shaper - switch between 1st and 2nd shaper stage	
Slow Shaper peaking time (ns)		90 / 180 / 250 ns		90 ns	
Fast shaper peaking time (ns)		40 ns		40 ns	
Shaper core GBW		1.51GHz		1.91 GHz	
Internal CSA bias filtering		✓		✓	
Calibration		External calibration pulse via pad			
		Internal calibration pulse – both charge polarities (square wave)			
		Internal calibration pulse – pseudo-single charge polarity (slow discharge)			
Area		0,093μm ²		0.146 μm ²	
Power consumption		8.7 mW		13.7 mW	
ENC (clean PS, internal filtering, no input capacitance)		278.2 e ⁻ rms	275.9 e ⁻ rms	309 e ⁻ rms	327.6 e ⁻ rms
VDDM-to-output gain (postlayout for e ⁻)					
@ 50 Hz		-108.30 dB		-132.70 dB	
@ 100 Hz		-100.40 dB		-120.70 dB	
@ 10 kHz		-23.68 dB		-40.87 dB	
@ 100 kHz		6.40 dB		-8.88 dB	

Core amplifier architecture in SE and DIFF channels almost identical for ENC level comparison taking into account power dissipation.

Radiation-Hardened PLL for Rx/Tx PMAs

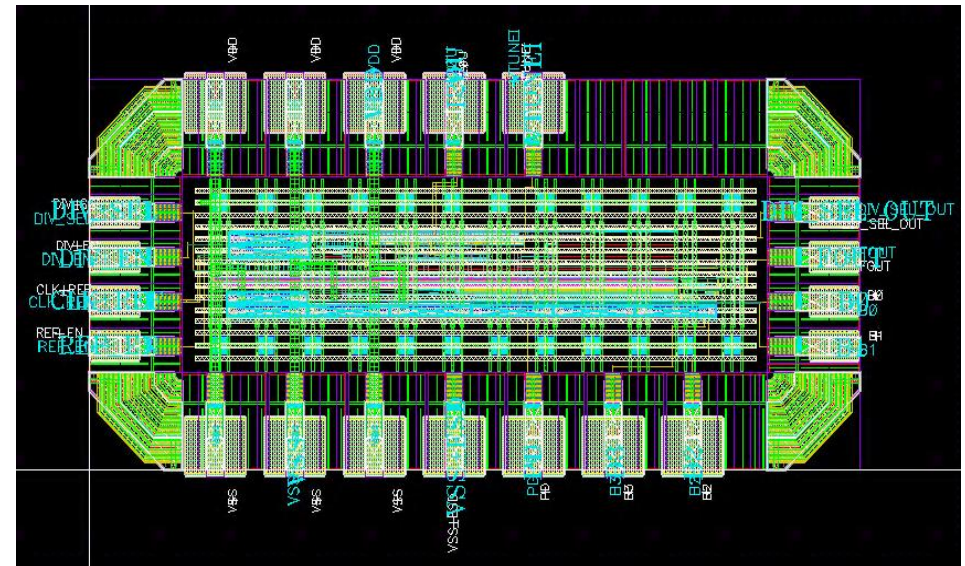
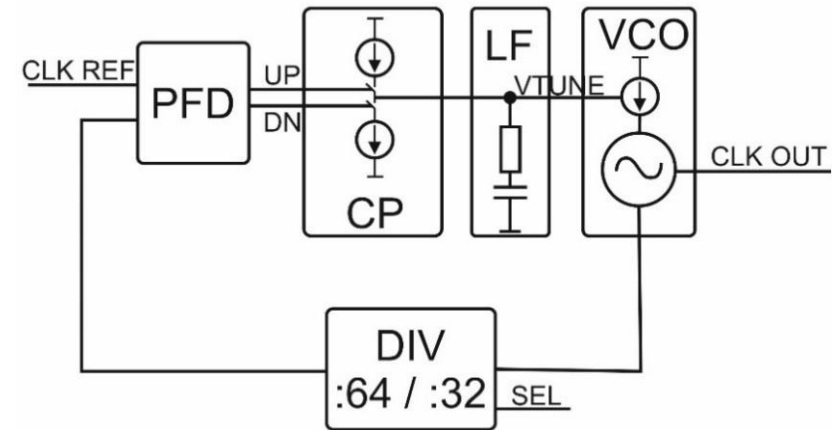
- 28 nm CMOS
- Area: 920 μm x 440 μm (without pads: 650 μm x 101 μm)
- Output frequency: **3.2 GHz** (reference frequency 50 MHz)

Selected techniques of radiation-hardening in:

- **Phase/Frequency Detector and frequency divider** - D flip-flops based on DICE architecture with C Muller elements,
- **Charge Pump** - „drain-switched” architecture
- **Voltage-Controlled Oscillator** - „unbalanced current starved” architecture

	Schematic	Postlayout
Output frequency	3.200 GHz	3.198 GHz
Period jitter p-p	1 ps	2.2 ps
rms period jitter p-p	0.5 ps	0.4 ps
Peak-minimum jitter	0.5 ps	0.9 ps

@fref = 50 MHz, divider 1/64. F_{out} (postlayout) = 3.198 GHz vs F_{out} (schematic) = 3.2 GHz.

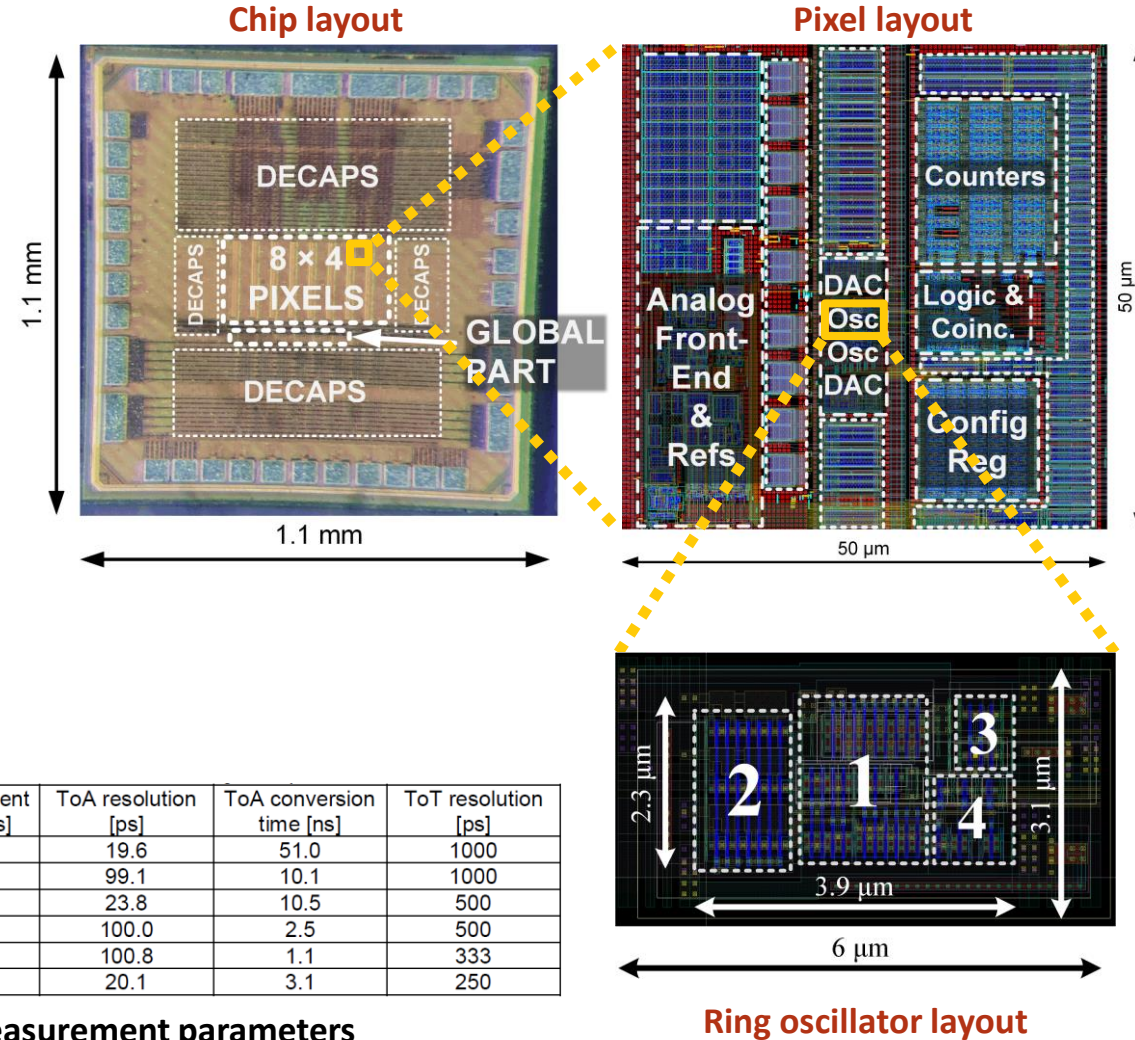


Prototype ROIC dedicated to the measurement of **time-of-arrival (ToA)** and **time-over-threshold (ToT)** with high resolution (expected ToA resolution on the order of tens of picoseconds).

- 28 nm CMOS technology
- 50 μm $\times$ 50 μm pixel size, 8 $\times$ 4 pixel matrix
- **Each pixel** includes inverter-based analog front-end with Zimmerman feedback, discriminator and **Vernier time-to-digital converter (TDC)** with two ring oscillators
- Pixel may operate either in time measurement mode (**ToA/ToT**), single photon counting (**SPC**) mode or oscillator calibration mode (reconfigurable 37-bit long counter/data shift register module per pixel)
- 60-bit pixel configuration register
- **Oscillator calibration** is performed using two global 8-bit DACs as well as in-pixel per-oscillator capacitance bank and 6-bit DAC

f_{Osc1} [GHz]	f_{Osc2} [GHz]	Fine ToA counter length [bits]	Measurement range [μs]	ToA resolution [ps]	ToA conversion time [ns]	ToT resolution [ps]
1	1.02	6	8.19	19.6	51.0	1000
1	1.11	4	8.19	99.1	10.1	1000
2	2.10	5	4.10	23.8	10.5	500
2	2.50	3	4.10	100.0	2.5	500
3	4.30	2	2.73	100.8	1.1	333
4	4.35	4	2.05	20.1	3.1	250

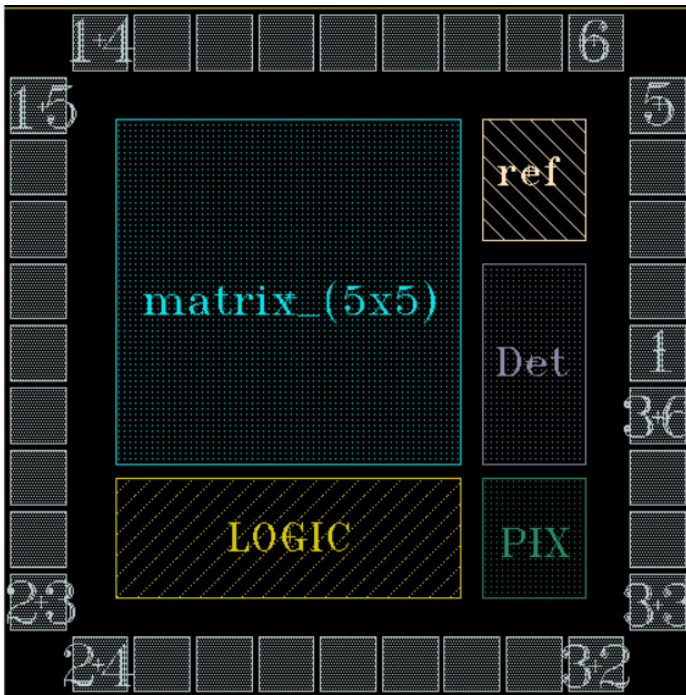
Expected measurement parameters



TECH-SMAUG-ND-1

Test Chip - Signal Measurements Using Noise Distribution

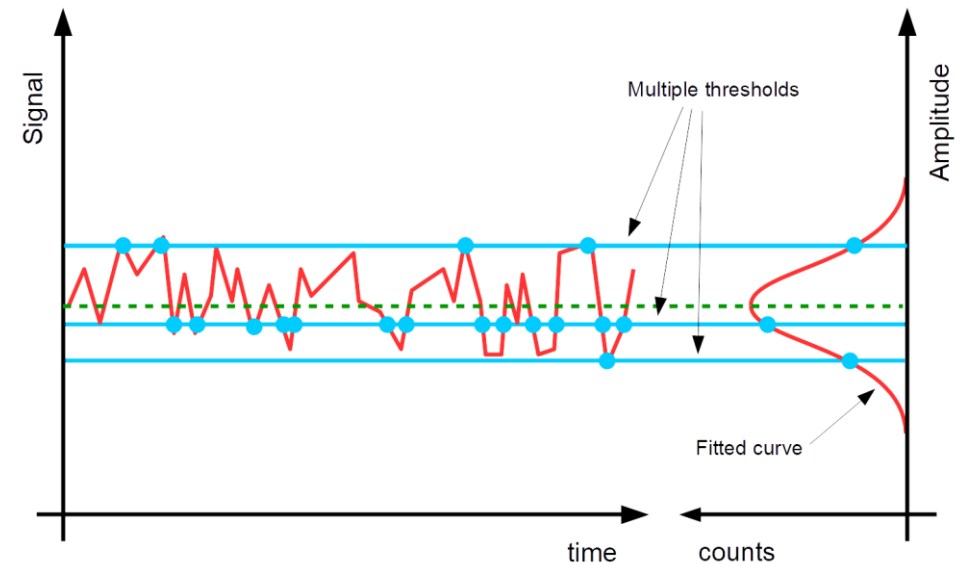
- CMOS 28nm
- 25 pixels, 100um pitch
- 6 comparators in each pixel
- Improving energy resolution providing "threshold scan" on a single pulse



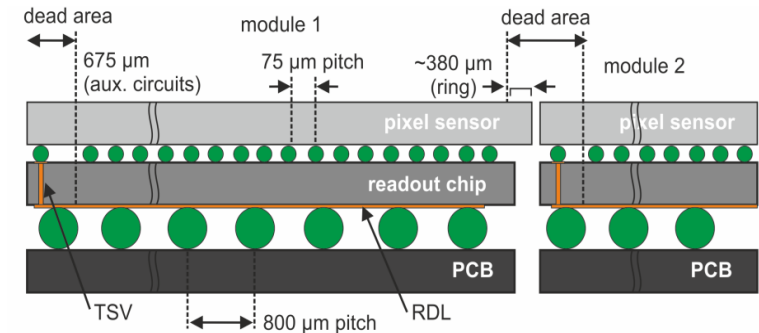
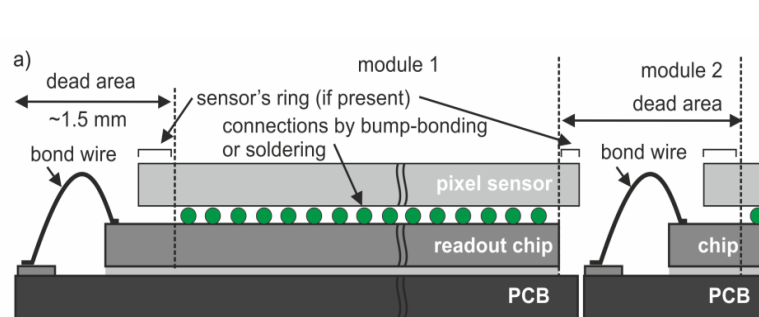
Signal measurements using noise distribution:

1. Use multiple, close-spaced thresholds
2. Count when noise cross the thresholds
3. Fit the distribution curve to the collected data

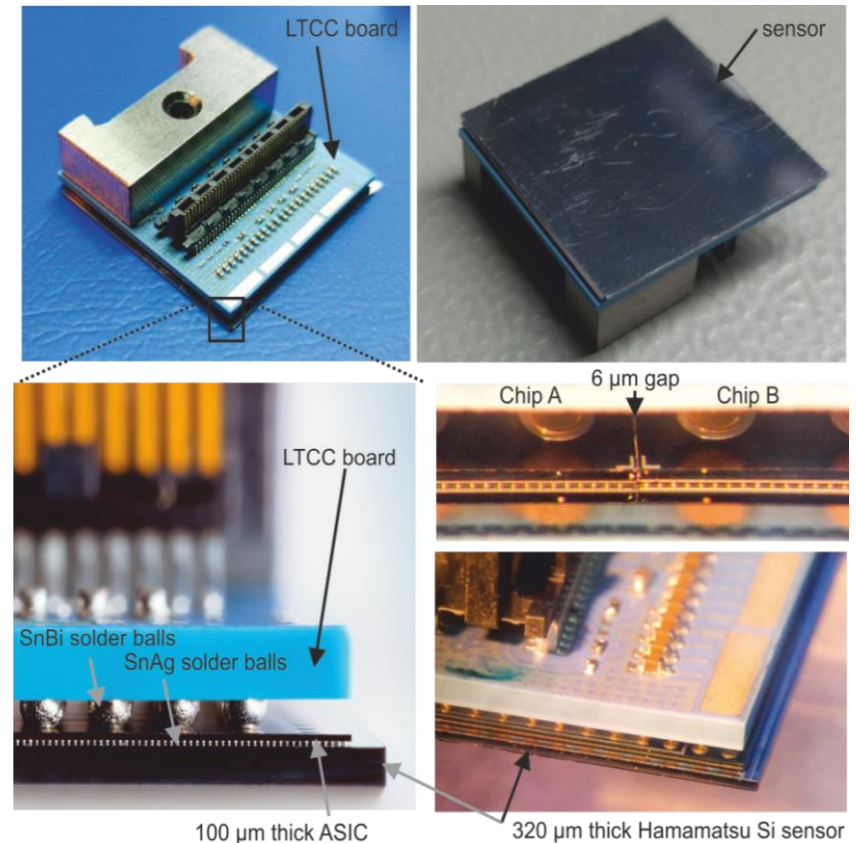
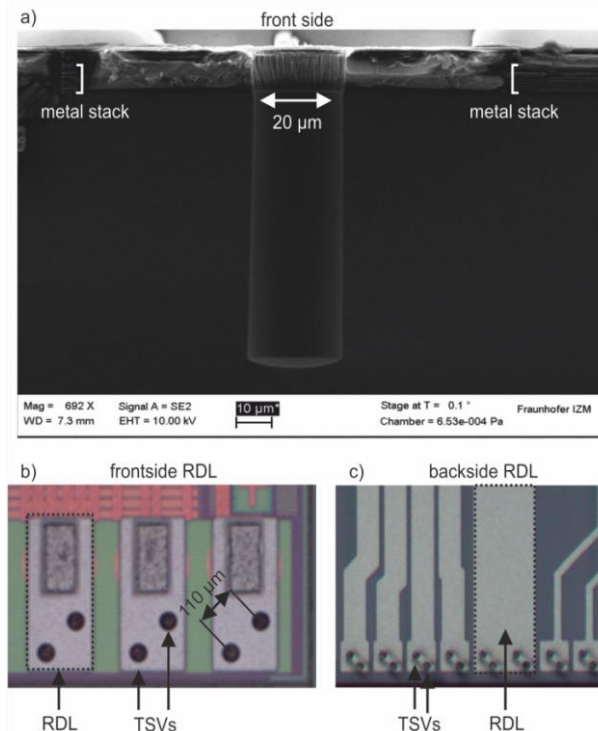
Thresholds spacing: $\sim \sigma_{\text{noise}}$



2-chip module with TSV with Si detector



TSV & backside RDL

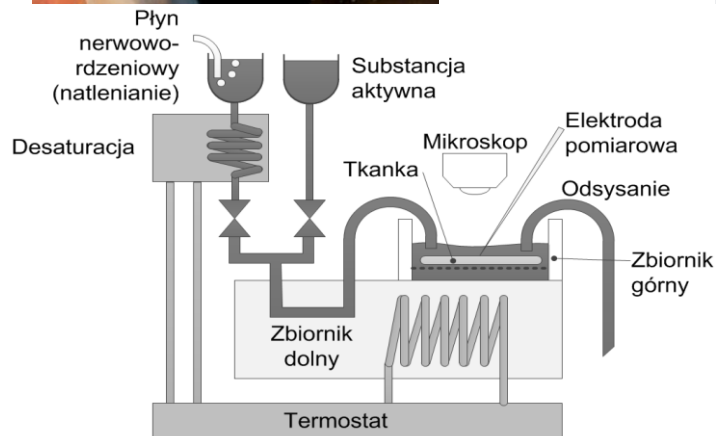
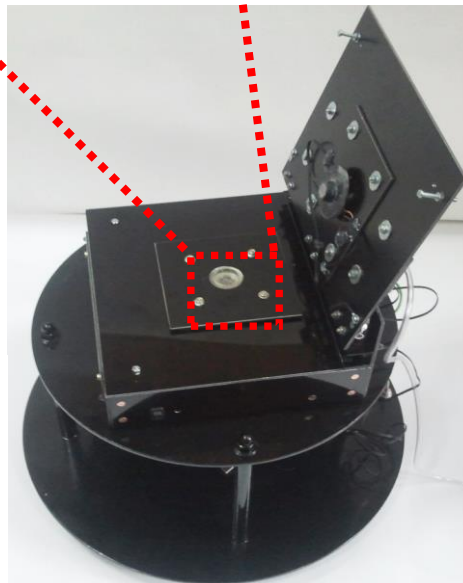
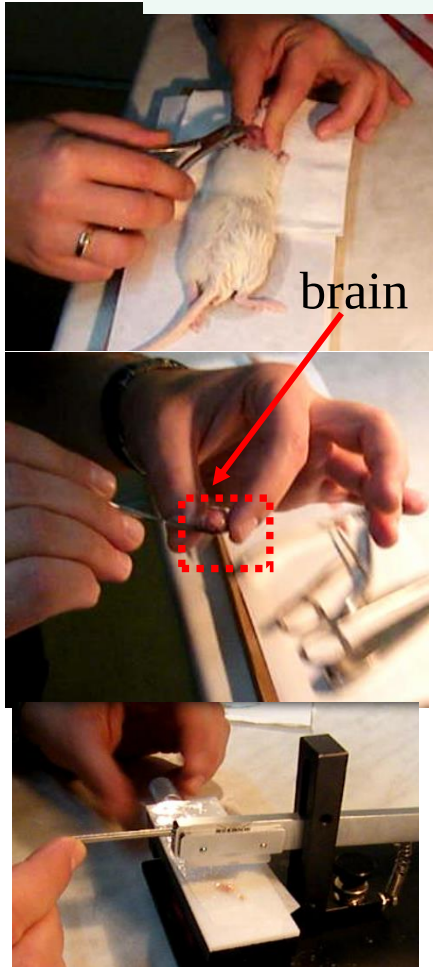


Neurobiology systems developed by our group

In vitro

University of Lodz

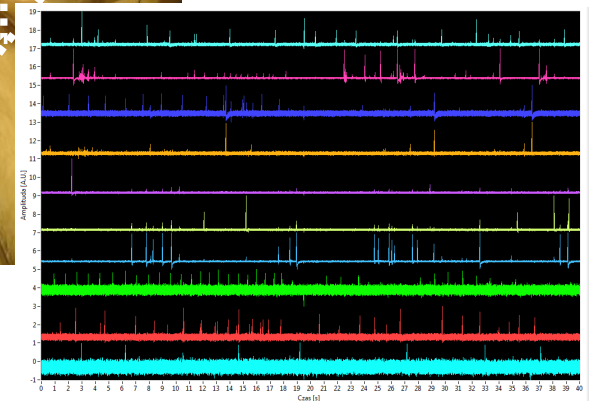
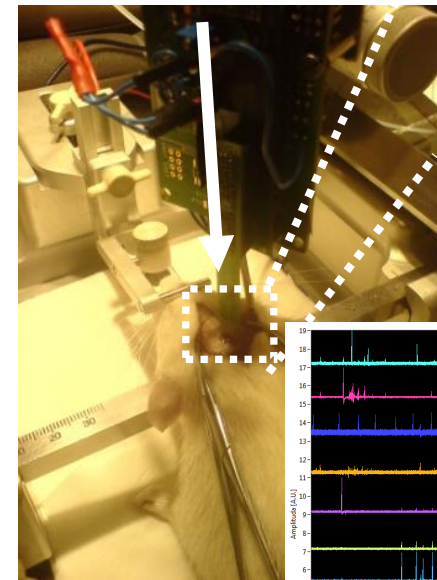
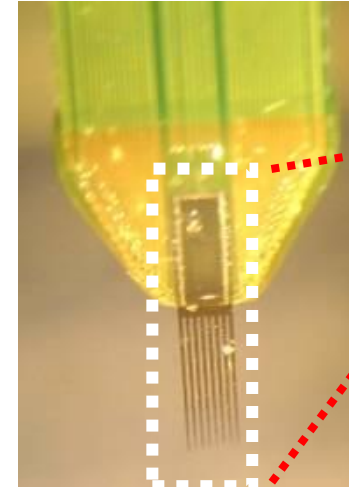
hippocampus



256/64 channel system for In Vitro experiments

In vivo

Jagiellonian University
in Cracow



64/16 channel system for In Vivo experiments

Neurobiological tests cooperation with Jagiellonian University

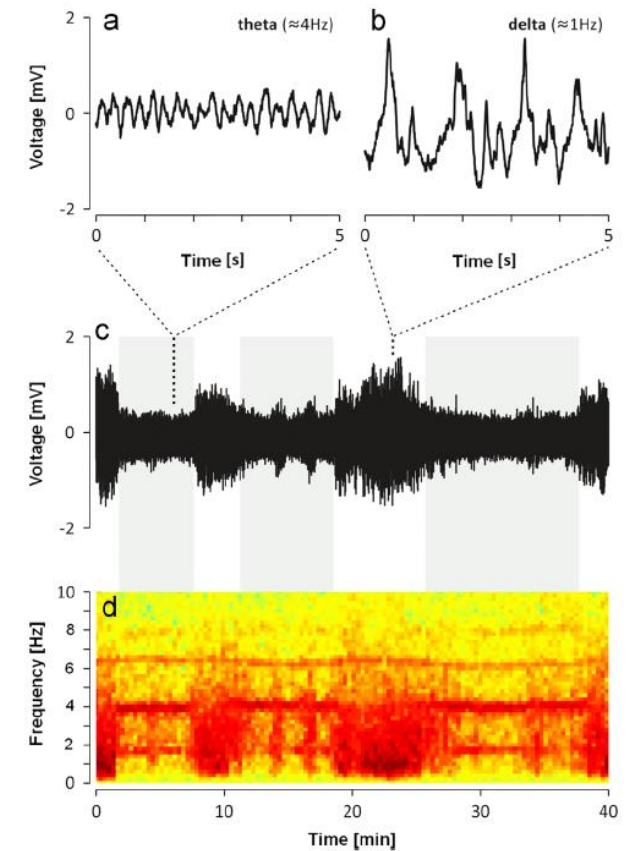
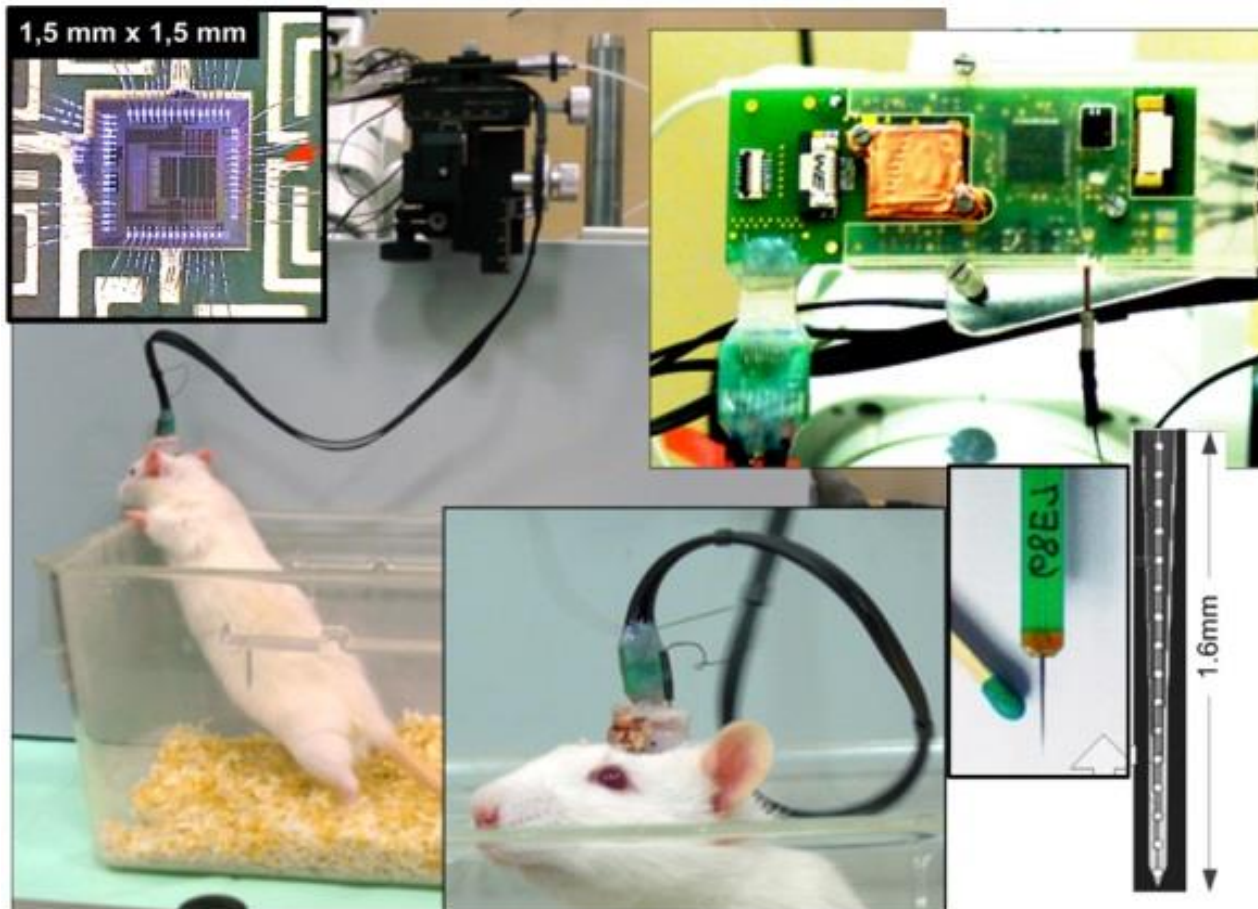
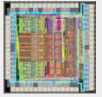
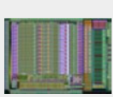
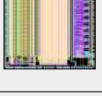
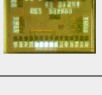
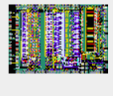
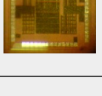
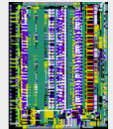
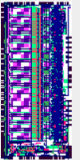
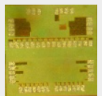
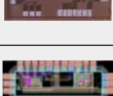
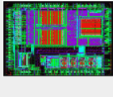
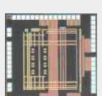
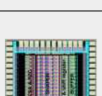
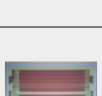
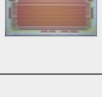
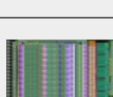


Fig. 14. An example showing the alternations of the dominant frequency of the local field potential (LFP) recorded in the nucleus incertus (NI) of the urethane anaesthetised rat. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

 ChSe Jr Technology: CMOS 40 nm Area: 2.0 mm x 4.5 mm Year(s): 2016 Place: DME, AGH UST, Cracow Description: Prototype high speed pixel chip for semiconductor detector readout.	 NRS D8 Technology: CMOS UMC 0.18 µm Area: 1.5 x 1.5 mm² Year(s): 2013 Place: DME, AGH UST, Cracow Description: 8-channel chip for recording and neural spike detection	 SXD2 Technology: CMOS austriamicrosystem 0.35 µm Area: 3 x 4.35 mm² Year(s): 2010 Place: DMI, AGH UST, Cracow Description: 32-channel photon counting chip for CdTe detector	 NEURO_A Technology: CMOS UMC 0.18 µm Area: 2.5 x 5 mm² Year(s): 2008 Place: DMI, AGH UST, Cracow Description: 64-channel readout ASIC for neurobiology experiments, architecture A Publications: [143] [180] [183] [185] [199] [202]
 STS/MUCH-XYTER2 Technology: UMC 180 nm CMOS MM/RF Area: 10 x 6.75 mm² Year(s): 2016 Place: DME, AGH UST, Cracow Description: A prototype 128-channel charge and amplitude measurement ASIC for the Silicon Tracking System and Muon Chamber detectors in the Compressed Baryonic Matter (CBM) experiment at FAIR, Germany.	 STSXYTER Technology: CMOS UMC 0.18 µm Area: 10 x 6.5 mm² Year(s): 2012 Place: DMI, AGH UST Cracow, ZITI Heidelberg Description: 128-channel time and amplitude digitalization chip for SSD with CBMnet interface	 RF2 Technology: CMOS UMC 0.18 µm Area: 0.75 x 1.5 mm² Year(s): 2010 Place: DMI, AGH UST, Cracow Description: prototype low-power RF transmitter	 RG64 Technology: CMOS austriamicrosystem 0.35 µm Area: 3.9 x 5 mm² Year(s): 2007 Place: DMI, AGH UST, Cracow Description: 64-channel fast single photon counting chip for Si strip detector Publications: [194] [195] [220]
 DS ToTIC2 Technology: CMOS UMC 180 nm Area: 1.5 x 1.5 mm² Year(s): 2014 Place: DME, AGH UST, Cracow Description: 8-channel dual-stage processing stage for silicon strip detectors with two-stage reset and on-chip reference DACs	 NeuroRf2 Technology: CMOS UMC 0.18 µm Area: 1.5 x 1.5 mm² Year(s): 2012 Place: DMI, AGH UST, Cracow Description: 2 versions of Rf transmitter and adc converter for SoC for multichannel neural signal activity monitoring	 ADC_10B Technology: CMOS UMC 0.18 µm Area: 0.75 x 1.5 mm² Year(s): 2010 Place: DMI, AGH UST, Cracow Description: 10-bit ADC Publications: [150] [162]	 FX24 Technology: CMOS austriamicrosystem 0.35 µm Area: 3.6 x 2.5 mm² Year(s): 2005-2006 Place: DNE, AGH UST, Cracow Description: 24- channels of fast frond-end electronics with new PZC circuit, fast shaper and two discriminators per channel, internal correction circuit. Control logic, counters, RAM, LVDS, testing circuits. Publications: [209]
 N100 Technology: CMOS UMC 180 nm Area: 5 x 5 mm² Year(s): 2014 Place: DME, AGH UST, Cracow Description: 100-channel chip for stimulation, recording and neural spike detection	 NeuAng01 Technology: CMOS UMC 0.18 µm Area: 1.5 x 1.5 mm² Year(s): 2012 Place: DMI, AGH UST, Cracow Description: 8 signal conditioning channels for SoC for multichannel neural signal activity monitoring	 FPDR90 Technology: CMOS TSMC 90nm Area: 4 x 4 mm² Year(s): 2010 Place: DMI, AGH UST, Cracow Description: Prototype of fast readout for silicon pixel detector, matrix 40 x 32 pixel of 100 x 100 µm² pixel size Publications: [139] [187] [189]	 DEDIX Technology: CMOS austriamicrosystem 0.35 µm Area: 3.9 x 5 mm² Year(s): 2005-2006 Place: DNE, AGH UST, Cracow Description: 64- channels of fast frond-end electronics with PZC circuit, shaper, two discriminators per channel, internal correction circuit. Control logic, counters, RAM, LVDS, testing circuits. Publications: [229] [255] [258] [262]
 UFCXv2 Technology: CMOS TSMC 130 nm Area: 10 x 20 mm² Year(s): 2014 Place: DME, AGH UST, Cracow Description: Final chip	 NeuDig02 Technology: CMOS UMC 0.18 µm Area: 1.5 x 1.5 mm² Year(s): 2012 Place: DMI, AGH UST, Cracow Description: 4 versions of rectifiers, LDO, bandgap, RAM memory & 4GHz RF transmitter for SoC for multichannel neural signal activity monitoring Publications: [128]	 NRTs Technology: CMOS UMC 0.18 µm Area: 1.5 x 1.5 mm² Year(s): 2009 Place: DMI, AGH UST, Cracow Description: 4 versions of Rf transmitter for SoC for multichannel neural signal activity monitoring	 NEUROPLAT Technology: CMOS Alcatel-Mietec 0.5 µm Area: 2.9 x 6.5 mm² Year(s): 2003-2004 Place: DNE, AGH UST, Cracow Description: 64-channels with AC-coupling at the input, low noise preamplifier, new concept of pass-band filters, analog multiplexer, control block, shift registers and LVDS, DACs Publications: [257] [286] [289]
 PIX40v2 Technology: CMOS TSMC 40 nm Area: 2.5 x 4 mm² Year(s): 2014 Place: DME, AGH UST, Cracow Description: Pixel matrix for X-ray detection with corrected C8P1 algorithm and low noise performance	 NeuDig01 Technology: CMOS UMC 0.18 µm Area: 1.5 x 1.5 mm² Year(s): 2011 Place: DMI, AGH UST, Cracow Description: controll circuit and adc converter for SoC for multichannel neural signal activity monitoring Publications: [163]	 RF_MZ Technology: CMOS UMC 0.18 µm Area: 1.5 x 1.5 mm² Year(s): 2009 Place: DMI, AGH UST, Cracow Description: 2 prototype low-power RF transmitters	 DTMROC Technology: CMOS 0.25 µm Area: 26 mm² Year(s): 2000-2003 Place: ATLAS Collaboration, CERN, Geneve Description: TDC with 3ns resolution, digital memory, command decoder, DACs, temperature sensor Publications: [230] [283] [320] [327]
 UFCXv1 Technology: CMOS TSMC 130 nm Area: 10 x 15 mm² Year(s): 2013 Place: DME, AGH UST, Cracow Description: Pixel prototype chip (NCRD project)	 NR8 Technology: CMOS UMC 0.18 µm Area: 1.5 x 1.5 mm² Year(s): 2011 Place: DMI, AGH UST, Cracow Description: 8-channel chip for recording biomedical signals Publications: [83]	 TOT_01 Technology: CMOS UMC 0.18 µm Area: 3 x 1.5 mm² Year(s): 2009 Place: DMI, AGH UST, Cracow Description: 31-channel front-end with ToT for SSD Publications: [140] [198]	 RX64DThv1 and RX64DThv2 Technology: CMOS austriamicrosystem 0.8 µm Area: 3.7 x 6.5 mm² Year(s): 2000-2002 Place: DNE, AGH UST, Cracow Description: 64-channel of low noise charge sensitive amplifier with shaper and two discriminators per channel. Pseudo-random counters, control logic, DACs, internal testing circuits. Publications: [267] [268] [276] [287] [290] [291] [292] [294]
 Pixel prototype 40 nm Technology: CMOS TSMC 40 nm Area: 2.5 x 4 mm² Year(s): 2013 Place: DME, AGH UST, Cracow Description: Pixel matrix for X-ray detection, C8P1 algorithm, Flash ADC	 FSDR16 Technology: CMOS UMC 0.18 µm Area: 1.5 x 1.5 mm² Year(s): 2011 Place: DMI, AGH UST, Cracow Description: 16-channel front-end with 5th order complex shaping amplifier Publications: [153] [156]	 PX90 Technology: CMOS TSMC 90nm Area: 4 x 4 mm² Year(s): 2009 Place: DMI, AGH UST, Cracow Description: First prototype of readout for silicon pixel detector, matrix 40 x 32 pixel of 100 x 100 µm² pixel size Publications: [179] [182] [204]	 BUSTUS Technology: CMOS Alcatec-Mietec 0.7 µm Area: 3.8 x 1.6 mm² Year(s): 2001-2002 Place: DNE, AGH UST, Cracow Description: Testing chip with low noise amplifiers with new concept of the filters Publications: [279] [307] [319]
 NSoCMZ1 Technology: CMOS UMC 0.18 µm Area: 5.0 x 5.0 mm² Year(s): 2013 Place: DME, AGH UST, Cracow Description: System On Chip for multichannel wireless neural signal recording	 NRS64 Technology: CMOS UMC 0.18 µm Area: 5 x 5 mm² Year(s): 2010 Place: DMI, AGH UST, Cracow Description: 64 signal conditioning channels for multichannel neural signal activity monitoring with stimulation and artifact reductions circuits Publications: [151] [142] [166]	 SXD64 Technology: CMOS austriamicrosystem 0.35 µm Area: 4.8 x 5 mm² Year(s): 2009 Place: DMI, AGH UST, Cracow Description: 64-channel photon counting chip for CdTe detector Publications: [159] [162] [200] [205]	 ABCD (several versions) Technology: BiCMOS 0.8 µm Area: 51 mm² Year(s): 1998-2002 Place: ATLAS Collaboration, CERN, Geneve Description: 128-channels readout for SSD working in SCT ATLAS detector Publications: [254] [264] [265] [265] [269] [282] [347] [347] [348] [354]
 DS ToTIC Technology: CMOS UMC 0.18 µm Area: 1.5 x 1.5 mm² Year(s): 2013 Place: DME, AGH UST, Cracow Description: 8-channel prototype dual stage processing stage for silicon strip detectors	 VIPIC – in collaboration with Fermilab Technology: 3D Tezzaron, CMOS CHRT 0.35 µm Area: 5.5 x 6.3 mm² x 2 Year(s): 2010 – in production Place: DMI, AGH UST, Cracow and FermiLab USA Description: 3D ASIC -Vertically Integrated Pixel Imaging Chip Publications: [186]	 NEURO_B Technology: CMOS UMC 0.18 µm Area: 2.5 x 5 mm² Year(s): 2008 Place: DMI, AGH UST, Cracow Description: 64-channel readout ASIC for neurobiology experiments, architecture B Publications: [180] [185] [199] [202]	
 ARF_ADC Technology: CMOS UMC 0.18 µm Area: 1.5 x 1.5 mm² Year(s): 2013 Place: DME, AGH UST, Cracow Description: 4-bit flash ADC for pixel systems, 6-bit flash ADC with comparator redundancy	 TOT_02 Technology: CMOS UMC 0.18 µm Area: 3 x 4.35 mm² Year(s): 2010 – in production Place: DMI, AGH UST, Cracow Description: 16-channel front-end with ToT & digital part for SSD Publications: [161]		
 AFE8 Technology: CMOS UMC 0.18 µm Area: 1.5 x 1.5 mm² Year(s): 2013 Place: DME, AGH UST, Cracow Description: 8 channel analog front-end readout chip dedicated for double-sided silicon microstrip sensors			